Qualcomm Technologies International, Ltd.

QCC3095 VFBGA

Production Information Data Sheet

80-74169-1 Rev. AA

March 8, 2024

Device description

- Quad-core processor architecture
- High-performance Bluetooth® stereo audio SoC
- Low power modes to extend battery life

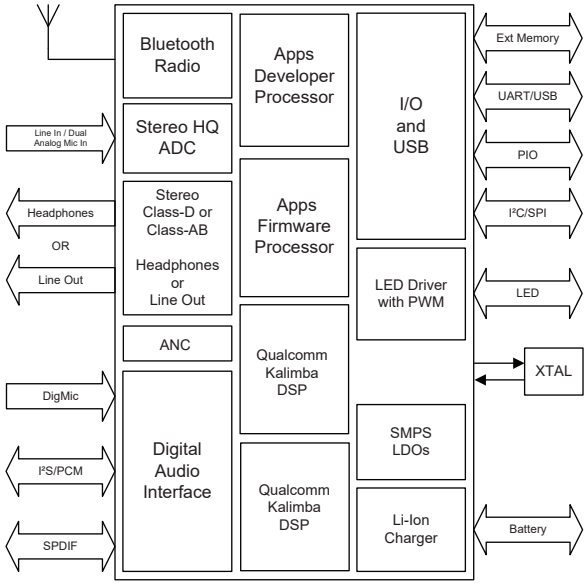
Applications

- Wireless speakers
- Wired/wireless stereo headsets/headphones

Features

- Qualified to Bluetooth v5.4 specification
- Dual 240 MHz Qualcomm® Kalimba™ audio DSP
- 32/80 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- Flexible LED controller and LED pins with PWM support
- Serial interfaces: UART, Bit Serializer (I²C/SPI), USB 2.0
- Advanced audio algorithms
- Active Noise Cancellation: Hybrid, Feedforward, and Feedback modes, using Digital or Analog Mics, enabled using license keys available from Qualcomm®
- Qualcomm® aptX™ and aptX HD Audio
- aptX Adaptive, enabled using license key
- 1 or 2 mic Qualcomm® cVc™ headset speech processing or 1-mic cVc speaker noise reduction and echo cancellation technology
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- 134-ball 6.7 mm x 7.4 mm x 1.0 mm, 0.5 mm pitch VFBGA

System architecture



QCC3095 VFBGA description

QCC3095 VFBGA is a system on-chip (SoC) with:

- On-chip Bluetooth
- Audio and programmable application processor
- High-performance, analog, and digital audio codecs
- Class-AB and Class-D digital-to-analog converter (DAC)
- Advanced power management
- Li-ion battery charger
- LED drivers
- Flexible interfaces, including:
  - I²S
  - I²C
  - UART
  - PIO

Processors

QCC3095 VFBGA includes an application-dedicated Developer Processor and a system Firmware Processor that run code from an external quad serial peripheral interface (QSPI) flash.

Both processors have tightly coupled memory (TCM) and an on-chip cache for performance while executing from external flash memory. The system Firmware Processor provides functions developed by Qualcomm Technologies International, Ltd. (QTIL). The Developer Processor provides flexibility to the product designer to customize their product.

Audio subsystem

The Audio subsystem contains two programmable Kalimba cores running Qualcomm® Kymera™ system DSP architecture framework from read only memory (ROM). A range of audio processing capabilities are provided from ROM, which are configurable in fully flexible audio graphs.

IDE/Software Development Tools

QCC3095 VFBGA is driven by a flexible software platform with integrated development environment (IDE) support.

For more information on development tools and the audio development kit (ADK) for the QCC3095 VFBGA, including information on Bluetooth and other features supported, go to www.qualcomm.com.

Ordering information

Device	Package			Order number
	Type	Size	Shipment method	
QCC3095 VFBGA	VFBGA 134-ball (Pb free)	6.7 mm x 7.4 mm x 1.0 mm 0.5 mm pitch	Tape and reel	QCC-3095-0-CSP134A-TR-06-0

NOTE Your attention is drawn to QTIL's Terms of Supply, see http://www.qualcomm.com/salesterms or please request a copy), in particular the section covering Product Warranties and Disclaimers. Please note that the product warranty differs for production, pre-production, and other versions.

Production status minimum order quantity is 4 kpcs.

Supply chain: QTIL's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

QCC3095 VFBGA Development Kit ordering information

The QCC3095 VFBGA Development Kit includes:

- A flexible development board with a wide range of interconnects
- QCC3095 VFBGA mounted on a plug-in module

TRBI200 is a high-speed universal serial bus (USB) to transaction bus interface that supports high-speed debug and flash programming, see *Related Information*.

This development equipment is available from QTIL using the following ordering information:

Description	Order number
QCC3095 VFBGA development kit including QCC3095 VFBGA module board	Full Kit: DK-QCC3095-VFBGA134-A-0 / SODIMM Only: DB-QCC3095-VFBGA134-A-0
TRBI200 Transaction Bridge Interface High-Speed Debug Adaptor and Programmer	DK-TRBI200-CE684-1

NOTE TRBI200 use is not mandatory for flash programming or other manufacturing operations. These actions are possible using direct USB connection to the QCC3095 VFBGA USB device interface.

Related Information

"Transaction bridge" on page 68

QTIL contacts

General information	http://www.qualcomm.com
Sales information	qcsales@qti.qualcomm.com
Compliance and standards	product.compliance@qti.qualcomm.com

QCC3095 VFBGA device details

Audio subsystem

- Dual 32-bit Kalimba audio digital signal processor (or processing) (DSP) cores with flexible clocking from 2 MHz to 240 MHz to enable optimization of performance vs. power consumption
- DSP executes code from ROM
- 384 KB program random access memory (RAM)
- 1408 KB data RAM

Application subsystem

- Dual-core application subsystem 32/80 MHz operation
- 32-bit Firmware Processor (reserved for system use) executes:
  - Bluetooth upper stack
  - Profiles
  - House-keeping code
- 32-bit Developer Processor executes:
  - Developer applications
- Both cores execute code from external flash memory using QSPI clocked at 32 MHz or 80 MHz
- On-chip caches per core enable optimized performance and power consumption

Bluetooth subsystem

- Qualified to Bluetooth v5.4 specification including 2 Mbps Bluetooth Low Energy and Bluetooth Low Energy Isochronous Channels
- Qualcomm® Bluetooth High Speed Link
- Single ended antenna connection with on-chip balun and Tx/Rx switch
- Bluetooth, Bluetooth Low Energy, and mixed topologies supported
- Class 1 support

Li-ion battery charger

- Integrated battery charger supporting:
  - Internal mode (up to 200 mA)
  - External mode (up to 1.8 A)
- Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V
- Thermal monitoring and management are available in application software
- Pre-charge to fast charge transition configurable at 2.5 V, 2.9 V, 3.0 V, and 3.1 V

Power management

- Integrated power management unit (PMU) to minimize external components
- QCC3095 VFBGA runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)
- Auto-switching between battery and USB (or other) charging source
- Power islands employed to optimize power consumption for variety of use-cases
- Dual switch-mode power supply (SMPS):
  - Automatic mode selection to minimize power consumption
  - 1.8 V SMPS generates power for both the device and off-chip circuits
  - Dedicated digital SMPS (output voltage changes automatically to minimize device power consumption)

Audio engine and digital audio interfaces

- 24-bit inter-integrated circuit sound (I²S) interface with 1 input and 3 output interfaces
- Programmable audio master clock (MCLK)
- Sony/Philips digital interface (SPDIF): Two instances configurable as input or output
- Stereo analog outputs configurable as differential Class-AB headphone outputs or differential high efficiency Class-D outputs:
  - Class-AB signal-to-noise ratio (SNR): 120.0 dB typ (Quiet mode).
  - Class-AB total harmonic distortion plus noise (THD +N): -91.1 dB typ.
  - Class-D SNR: 105.1 dB typ.
  - Class-D THD+N: -90.1 dB typ.
- Quad analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs:
  - SNR differential: 99.2 dB typ.
  - THD+N differential: -95.0 dB typ.
- 1 microphone bias (single bias shared by four channels):
  - Crosstalk attenuation between two inputs using recommended application circuit: 80 dB typ.
- Digital microphone inputs with capability to interface up to 10 digital microphones
- Both analog-to-digital converter (ADC)s and DACs support sample rates of 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz. DACs also support 192 kHz and 384 kHz.

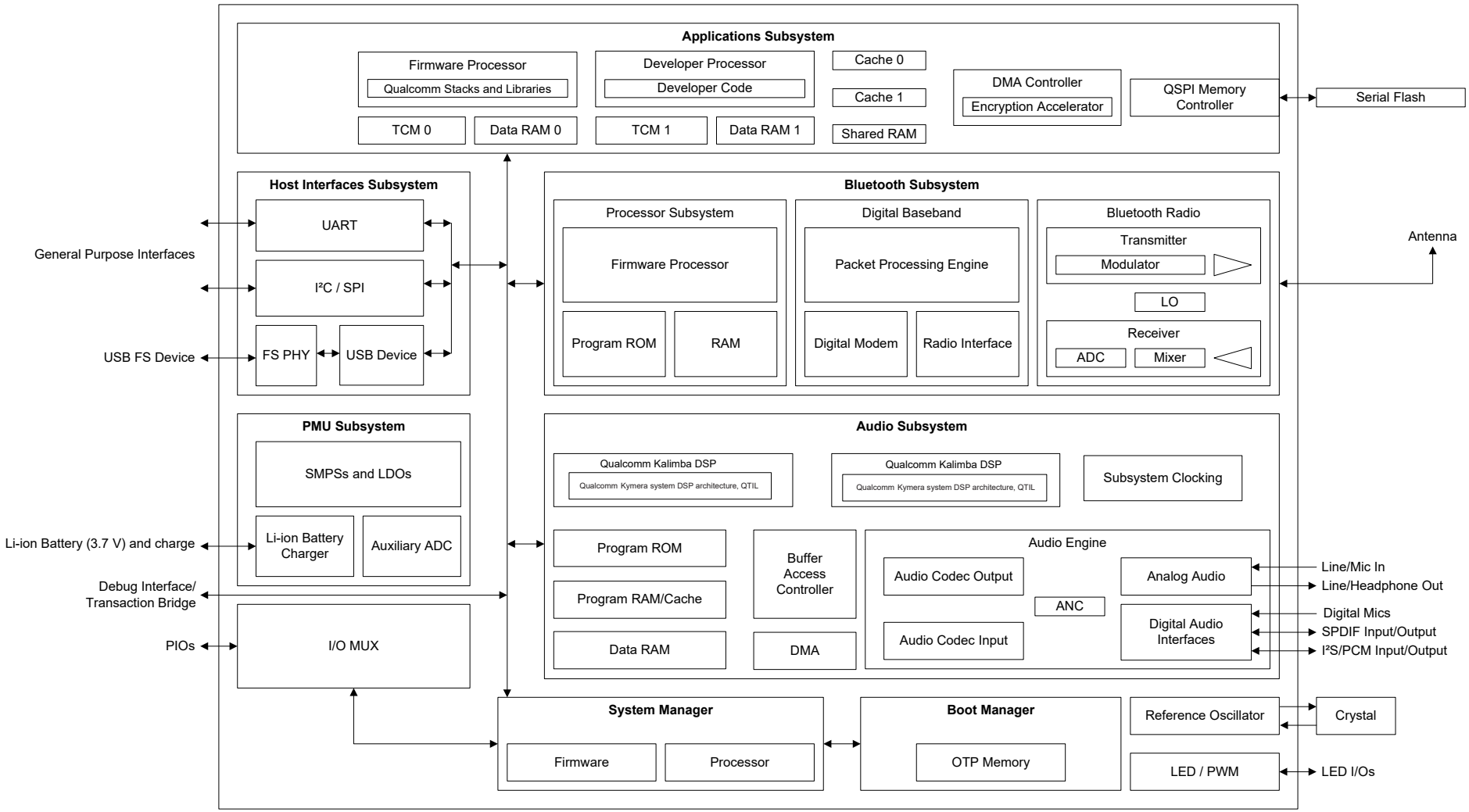
Peripherals and physical interfaces

- A universal asynchronous receiver transmitter (UART) interface
- 3 x Bit Serializers (programmable serial peripheral interface (SPI) and inter-integrated circuit interface (I²C) hardware accelerator)
- 1 x USB interface:
  - A full speed USB (USB-FS) Device (12 Mbps)
- QSPI NOR flash interface
  - QSPI encryption to protect developer code and data
  - Encryption programmable with a 128-bit security key of original equipment manufacturer (OEM) choice stored in on-chip one-time programmable (OTP) memory
- Up to 53 programmable input/output (PIO) and 6 open drain/digital input light-emitting diode (LED) pads with pulse width modulation (PWM)

Package and compliance

- 134-ball 6.7 mm x 7.4 mm x 1.0 mm, 0.5 mm pitch VFBGA
- Green (restriction of hazardous substances (RoHS) compliant, and no antimony or halogenated flame retardants)

QCC3095 VFBGA functional block diagram



QCC3095 VFBGA functional block diagram

Revision history

Revision	Date	Change reason
AA	March 2024	Initial release.

Status information

QTIL Product Data Sheets progress according to the following formats: Advance Information, Engineering Sample, Pre-production Information, and Production Information. The status of this document is **Production Information**.

Advance Information

Information for designers concerning QTIL product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

Engineering Sample

Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by QTIL without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalized. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by QTIL without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Device implementation

As the feature-set of the QCC3095 VFBGA is firmware build-specific, see the relevant software release note for the exact implementation of features on the QCC3095 VFBGA.

Life support policy and use in safety-critical applications

QTIL products are not authorized for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. QTIL will not warrant the use of its devices in such applications.

Contents

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1 Package information

QCC3095 VFBGA is available in a 6.7 mm x 7.4 mm x 1.0 mm 134-ball VFBGA package.

1.1 Chip marking

Chip marking identifies lot-specific information about QCC3095 VFBGA.

Figure 1-1 shows the product marking for QCC-3095-0-CSP134A-TR-06-0 in a 134-ball 6.7 mm x 7.4 mm x 1.0 mm VFBGA package.

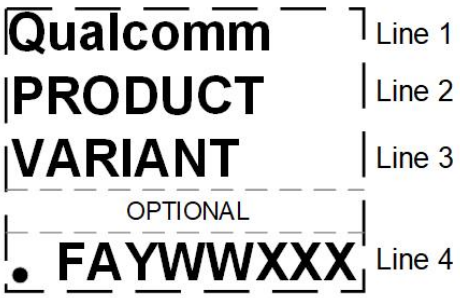


Figure 1-1 QCC3095 VFBGA chip marking

NOTE Figure 1-1 is not to scale. The marking font and image are for illustration purposes only.

The circle location mark identifies pin 1.

Table 1-1 QCC3095 VFBGA chip marking content

Line	Description	Definition
1	Qualcomm text	-
2	Product name	QCC3095
3	Config, revision, and feature codes	005
Optional extra trace information	Imaginary box bounded by marking area width and one line space below Line 3 and one line space above Line 4	-
4	Manufacturing trace code	FAYWWXXX ■ F: Foundry company code ■ A: Assembly site code ■ Y: Year ■ WW: Work week ■ XXX: Lot serial number

1.2 QCC3095 VFBGA package dimensions diagram

Figure 1-2 shows the dimensions of the QCC3095 VFBGA package from top, bottom, and side views.

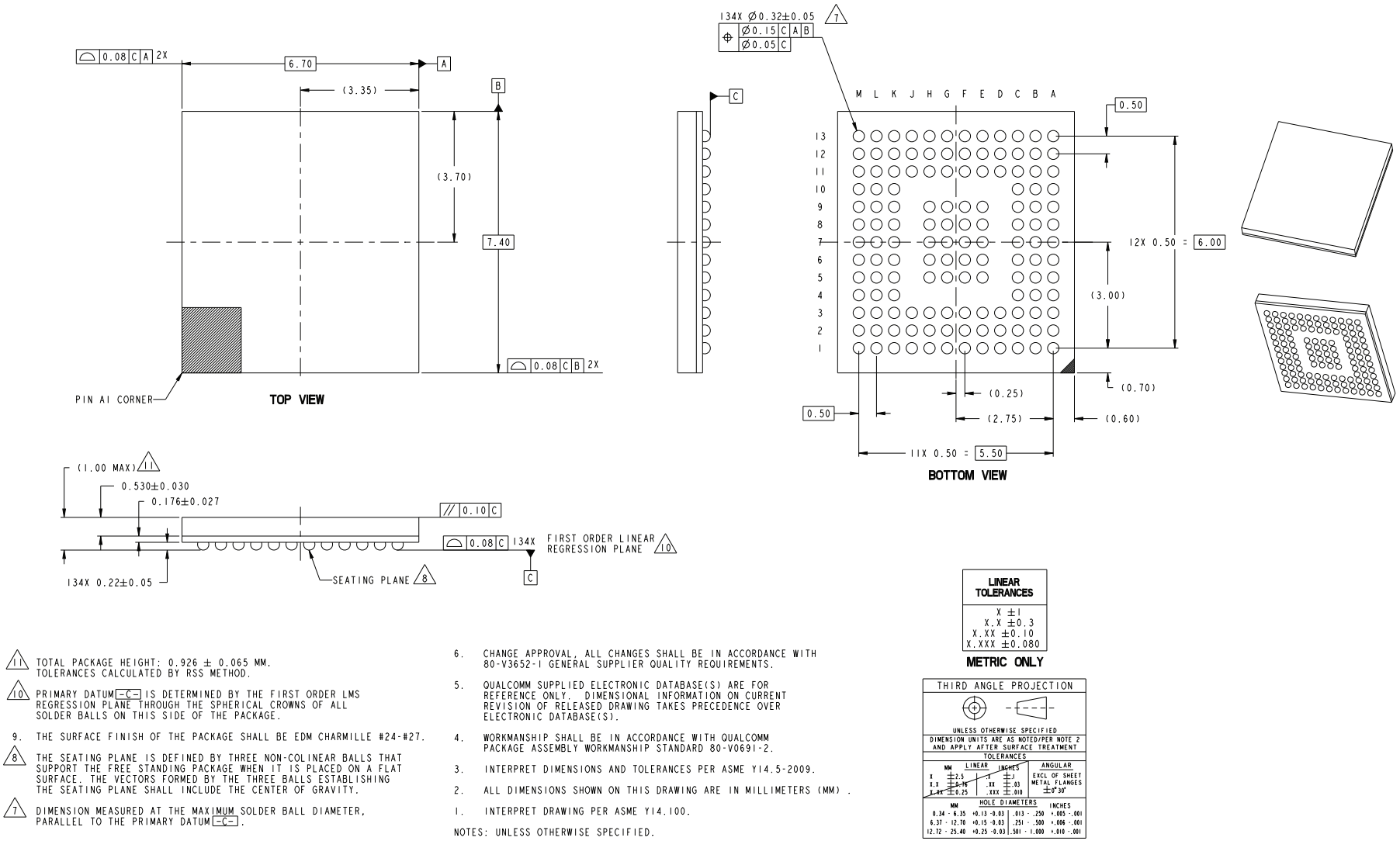


Figure 1-2 QCC3095 VFBGA package dimensions diagram

1.3 QCC3095 VFBGA pin allocations

Table 1-2 QCC3095 VFBGA pin allocations (Orientation from top of device)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	VDD_AUX	XTAL_OUT	XTAL_IN	AUDIO_MIC3_N/LINEIN_3_N	AUDIO_MIC3_P/LINEIN_3_P	AUDIO_MIC1_P/LINEIN_1_P	AUDIO_MIC1_N/LINEIN_1_N	VDD_AUDIO_1V8	AUDIO_MIC_BIAS	VSS_AUDIO_HP_SPK1	VDD_AUDIO_HP_SPK1	VDD_AUDIO_HP_SPK2	VSS_AUDIO_HP_SPK2	**A**
B	VDD_XTAL_1V8	XTAL_CLKOUT	VSS_XTAL_OSC	AUDIO_MIC4_P/LINEIN_4_P	AUDIO_MIC4_N/LINEIN_4_N	AUDIO_MIC2_P/LINEIN_2_P	AUDIO_MIC2_N/LINEIN_2_N	VSS_AUDIO_REF	AUDIO_BGBYP	AUDIO_HP1_P/SPK1_P	AUDIO_HP1_N/SPK1_N	AUDIO_HP2_N/SPK2_N	AUDIO_HP2_P/SPK2_P	**B**
C	VSS_BT	VSS_BT	VSS_AUX	VSS_AUDIO	VSS_AUDIO	VSS_AUDIO	VSS_AUDIO	VSS_AUDIO	PIO[23]	PIO[22]	PIO[52]	PIO[53]	VDD_PADS_4	**C**
D	BT_RF	VSS_BT	VSS_BT								PIO[24]	PIO[25]	VDD_PADS_7	**D**
E	VSS_BT	VSS_BT	VDD_BT_RADIO		PIO[35]	PIO[45]	PIO[49]	PIO[51]	PIO[50]		PIO[47]	PIO[48]	VDD_PADS_7	**E**
F	VDD_BT_1V8	VDD_PADS_6	PIO[37]		PIO[34]	PIO[40]	VSS_DIG_PADS	VSS_DIG_PADS	PIO[7]		PIO[1]	PIO[5]	PIO[46]	**F**
G	PIO[38]	PIO[39]	PIO[36]		PIO[44]	PIO[41]	VSS_DIG_PADS	VSS_DIG_PADS	PIO[2]		PIO[8]	PIO[6]	VDD_PADS_1	**G**
H	QSPI1_IO[3]	QSPI1_CS0#	PIO[16]		PIO[43]	PIO[42]	PIO[27]	AIO[1]/LED[1]	AIO[2]/LED[2]		PIO[4]	PIO[3]	SMPS_VCHG	**H**
J	VDD_PADS_2	QSPI1_IO[1]	PIO[21]								AIO[5]/LED[5]	AIO[4]/LED[4]	LX_1V8	**J**
K	QSPI1_IO[0]	QSPI1_CLK	PIO[18]	PIO[19]	PIO[28]	PIO[32]	SYS_CTRL	CHG_EXT	AIO[3]/LED[3]	AIO[0]/LED[0]	VSS_PMU	VSS_PMU	VSS_SMPS_1V8	**K**
L	QSPI1_IO[2]	PIO[20]	PIO[17]	PIO[31]	PIO[29]	USB_DN	USB_DP	VDD_VKA	VCHG_SENSE	VBAT_SENSE	VDD_BYP	VSS_PMU	VSS_SMPS_DIG	**L**
M	VDD_PADS_3	PIO[15]	VDD_PADS_5	PIO[26]	PIO[30]	PIO[33]	VDD_DIG	VDD_PMU_VINDIG	VBAT	VDD_BYP_CHG	SMPS_DCPL	SMPS_VBAT	LX_DIG	**M**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	

1.4 QCC3095 VFBGA device terminal functions

The balls on the QCC3095 VFBGA are grouped into various terminal functions. The device terminal functions include:

- Radio
- Clock
- USB
- QSPI
- PIO
- Audio
- AIO/LED drivers
- SMPS
- Power supplies and control
- Ground

1.4.1 Radio device terminal functions

Table 1-3 QCC3095 VFBGA Radio device terminal functions

Radio	Ball	Pad type	Supply domain	Description
BT_RF	D1	RF	VDD_BT_RADIO	Bluetooth transmit/receive.

1.4.2 Clock device terminal functions

Table 1-4 QCC3095 VFBGA Clock device terminal functions

Clock	Ball	Pad type	Supply domain	Description
XTAL_IN	A3	Analog	Internal 0.95 V from VDD_XTAL_1V8	XTAL clock input.
XTAL_OUT	A2			XTAL clock output.
XTAL_CLKOUT	B2		VDD_XTAL_1V8	Buffered clock output.

1.4.3 USB device terminal functions

Table 1-5 QCC3095 VFBGA USB device terminal functions

USB	Ball	Pad type	Supply domain	Description
USB_DN	L6	Digital	VDD_BYP	USB Full Speed device D- I/O.
USB_DP	L7			USB Full Speed device D+ I/O.

1.4.4 QSPI device terminal functions

Table 1-6 QCC3095 VFBGA QSPI device terminal functions

QSPI	Ball	Pad type	Supply domain	Reset state	Description
QSPI1_IO[3]	H1	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_2	Strong pull-up	QSPI 1, input/output 3.
QSPI1_IO[2]	L1			Strong pull-up	QSPI 1, input/output 2.
QSPI1_IO[1]	J2			Weak pull-down	QSPI 1, input/output 1.
QSPI1_IO[0]	K1			Weak pull-down	QSPI 1, input/output 0.
QSPI1_CLK	K2			Strong pull-down	QSPI 1, clock output.
QSPI1_CS0#	H2			Strong pull-up	QSPI 1, chip select 0, active low.

1.4.5 PIO device terminal functions

NOTE PIO alternative functions include SPI/I²C, UART, SPDIF, and digital microphone. Any PIO function can be multiplexed to any PIO. Table 1-7 shows that alternative functions are available only on the specific PIO port.

Table 1-7 QCC3095 VFBGA PIO device terminal functions

PIO port	Ball	Pad type	Supply domain	Reset state	Description
PIO[53]	C12	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_4	Weak pull-down	Programmable I/O line 53.
PIO[52]	C11				Programmable I/O line 52.
PIO[51]	E8	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_7	Weak pull-down	Programmable I/O line 51.
PIO[50]	E9				Programmable I/O line 50.
PIO[49]	E7				Programmable I/O line 49.
PIO[48]	E12				Programmable I/O line 48.
PIO[47]	E11				Programmable I/O line 47.
PIO[46]	F13				Programmable I/O line 46.
PIO[45]	E6	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_5	Strong pull-up	Programmable I/O line 45.
PIO[44]	G5				Programmable I/O line 44.
PIO[43]	H5			Weak pull-down	Programmable I/O line 43.
PIO[42]	H6			Strong pull-up	Programmable I/O line 42.
PIO[41]	G6			Strong pull-down	Programmable I/O line 41.
PIO[40]	F6			Weak pull-down	Programmable I/O line 40.
PIO[39]	G2	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_6	Strong pull-up	Programmable I/O line 39. Alternative function: ■ QSPI2_IO[3][a]
PIO[38]	G1				Programmable I/O line 38. Alternative function: ■ QSPI2_CS0#[a]
PIO[37]	F3			Weak pull-down	Programmable I/O line 37. Alternative function: ■ QSPI2_IO[1][a]

[a] QSPI2 is reserved for future use.

PIO port	Ball	Pad type	Supply domain	Reset state	Description
PIO[36]	G3	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_6	Strong pull-up	Programmable I/O line 36. Alternative function: ■ QSPI2_IO[2][a]
PIO[35]	E5			Strong pull-down	Programmable I/O line 35. Alternative function: ■ QSPI2_CLK[a]
PIO[34]	F5			Weak pull-down	Programmable I/O line 34. Alternative function: ■ QSPI2_IO[0][a]
PIO[33]	M6	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_5	Strong pull-up	Programmable I/O line 33.
PIO[32]	K6				Programmable I/O line 32.
PIO[31]	L4			Weak pull-down	Programmable I/O line 31.
PIO[30]	M5			Strong pull-up	Programmable I/O line 30.
PIO[29]	L5			Strong pull-down	Programmable I/O line 29.
PIO[28]	K5			Weak pull-down	Programmable I/O line 28.
PIO[27]	H7			Strong pull-up	Programmable I/O line 27.
PIO[26]	M4				Programmable I/O line 26.
PIO[25]	D12	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_4	Weak pull-down	Programmable I/O line 25.
PIO[24]	D11				Programmable I/O line 24.
PIO[23]	C9				Programmable I/O line 23. Alternative function: ■ PCM_DIN[2]
PIO[22]	C10				Programmable I/O line 22. Alternative function: ■ PCM_DIN[1]

PIO port	Ball	Pad type	Supply domain	Reset state	Description
PIO[21]	J3	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_3	Weak pull-down	Programmable I/O line 21. Alternative function: ■ PCM_DOUT[2]
PIO[20]	L2			Strong pull-up	Programmable I/O line 20. Alternative function: ■ PCM_DOUT[1]
PIO[19]	K4			Weak pull-down	Programmable I/O line 19. Alternative function: ■ PCM_DIN[0]
PIO[18]	K3			Strong pull-up	Programmable I/O line 18. Alternative function: ■ PCM_DOUT[0]
PIO[17]	L3			Weak pull-down	Programmable I/O line 17. Alternative function: ■ PCM_SYNC
PIO[16]	H3				Programmable I/O line 16. Alternative function: ■ PCM_CLK
PIO[15]	M2			Strong pull-up	Programmable I/O line 15. Alternative function: ■ MCLK_OUT
PIO[8]	G11	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_1	Weak pull-down	Programmable I/O line 8. Alternative function: ■ TBR_CLK
PIO[7]	F9			Strong pull-up[a]	Programmable I/O line 7. Alternative function: ■ TBR_MISO[0]
PIO[6]	G12			Strong pull-up	Programmable I/O line 6. Alternative function: ■ TBR_MOSI[0]

[a] PIO[7] must not be held low at boot.

PIO port	Ball	Pad type	Supply domain	Reset state	Description
PIO[5]	F12	Digital: Bidirectional with programmable strength internal pull-up/pull-down	VDD_PADS_1	Weak pull-down	Programmable I/O line 5. Alternative function: ■ TBR_MISO[1]
PIO[4]	H11				Programmable I/O line 4. Alternative function: ■ TBR_MOSI[1]
PIO[3]	H12			Strong pull-up	Programmable I/O line 3. Alternative function: ■ TBR_MISO[2]
PIO[2]	G9			Weak pull-down	Programmable I/O line 2. Alternative function: ■ TBR_MISO[3]
PIO[1]	F11			Strong pull-up[a]	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot. Alternative function: ■ Programmable I/O line 1

[a] PIO[1] is reconfigurable as a PIO after boot.

1.4.6 Audio device terminal functions

Table 1-8 QCC3095 VFBGA Audio device terminal functions

Audio	Ball	Pad type	Supply domain	Description
AUDIO_HP1_N/SPK1_N	B11	Analog	VDD_AUDIO_HP_SPK1	Headphone/speaker differential 1 output, negative.[a] Alternative function: ■ Differential line output 1, negative[a]
AUDIO_HP1_P/SPK1_P	B10			Headphone/speaker differential 1 output, positive.[a] Alternative function: ■ Differential line output 1, positive[a]
AUDIO_HP2_N/SPK2_N	B12		VDD_AUDIO_HP_SPK2	Headphone/speaker differential 2 output, negative.[a] Alternative function: ■ Differential line output 2, negative[a]
AUDIO_HP2_P/SPK2_P	B13			Headphone/speaker differential 2 output, positive.[a] Alternative function: ■ Differential line output 2, positive[a]
AUDIO_MIC_BIAS	A9		VDD_BYP	Mic bias output.
AUDIO_BGBYP	B9		VDD_AUDIO_1V8	Audio bandgap decoupling I/O.
AUDIO_MIC1_N/ LINEIN_1_N	A7			Microphone differential 1 input, negative. Alternative function: ■ Differential audio line input 1, negative
AUDIO_MIC1_P/ LINEIN_1_P	A6			Microphone differential 1 input, positive. Alternative function: ■ Differential audio line input 1, positive
AUDIO_MIC2_N/ LINEIN_2_N	B7			Microphone differential 2 input, negative. Alternative function: ■ Differential audio line input 2, negative
AUDIO_MIC2_P/ LINEIN_2_P	B6			Microphone differential 2 input, positive. Alternative function: ■ Differential audio line input 2, positive

[a] The polarity of the headphone/speaker differential outputs is swapped relative to mic/linein inputs.

Audio	Ball	Pad type	Supply domain	Description
AUDIO_MIC3_N/ LINEIN_3_N	A4	Analog	VDD_AUDIO_1V8	Microphone differential 3 input, negative. Alternative function: ■ Differential audio line input 3, negative
AUDIO_MIC3_P/ LINEIN_3_P	A5			Microphone differential 3 input, positive. Alternative function: ■ Differential audio line input 3, positive
AUDIO_MIC4_N/ LINEIN_4_N	B5			Microphone differential 4 input, negative. Alternative function: ■ Differential audio line input 4, negative
AUDIO_MIC4_P/ LINEIN_4_P	B4			Microphone differential 4 input, positive. Alternative function: ■ Differential audio line input 4, positive

1.4.7 AIO/LED drivers device terminal functions

NOTE Each AIO/LED driver is allocated its own PIO number.

Table 1-9 QCC3095 VFBGA AIO/LED drivers device terminal functions

AIO/LED drivers	PIO port	Ball	Pad type	Supply domain	Description
AIO[5]/ LED[5]	PIO[63]	J11	Analog or digital input/ open drain output.	VDD_BYP	General-purpose analog/digital input or open drain LED output.
AIO[4]/ LED[4]	PIO[62]	J12			
AIO[3]/ LED[3]	PIO[61]	K9			
AIO[2]/ LED[2]	PIO[60]	H9			
AIO[1]/ LED[1]	PIO[59]	H8			
AIO[0]/ LED[0]	PIO[58]	K10			

1.4.8 SMPS device terminal functions

Table 1-10 QCC3095 VFBGA SMPS device terminal functions

SMPSs	Ball	Pad type	Supply domain	Description
LX_1V8	J13	Analog	SMPS_DCPL	Inductor connection for 1.8 V SMPS.
LX_DIG	M13			Inductor connection for digital SMPS.

1.4.9 Power supplies and control device terminal functions

Table 1-11 QCC3095 VFBGA Power supplies and control device terminal functions

Power supplies and control	Ball	Pad type	Supply domain	Description
VDD_AUX	A1	Supply	-	1.8 V supply for AUX.
VDD_XTAL_1V8	B1			1.8 V supply for XTAL driver.
VDD_BT_RADIO	E3			Internally regulated supply for Bluetooth radio.
VDD_BT_1V8	F1			1.8 V supply for Bluetooth radio.
VDD_AUDIO_HP_SPK1	A11			1.8 V supply for HP/SPK1 output.
VDD_AUDIO_HP_SPK2	A12			1.8 V supply for HP/SPK2 output.
VDD_AUDIO_1V8	A8			1.8 V supply for analog audio.
VDD_DIG	M7			0.7/0.8/0.9 V supply output from digital regulator.

Power supplies and control	Ball	Pad type	Supply domain	Description
VDD_PMU_VINDIG	M8	Supply	-	1.8 V supply input into digital regulator.
VDD_VKA	L8			Low voltage supply output from keep-alive/dormant regulator.
SYS_CTRL	K7	Digital input	VBAT	Typically connected to an ON/OFF push button. If power is present from the battery and/or charger, and software has placed the device in the OFF or DORMANT state, a button press boots the device. Also usable as a digital input in normal operation. No pull. Additional function: ■ PIO[0] input only
VCHG_SENSE	L9	Analog	VCHG	Charger input sense pin after external mode sense-resistor. High impedance. **NOTE** If using internal charger or no charger, connect VCHG_SENSE direct to SMPS_VCHG.
CHG_EXT	K8			External charger transistor current control. Connect to base of external charger transistor as per application schematic.
VBAT_SENSE	L10		VBAT	Battery voltage sense input.
VBAT	M9	Supply	VBAT	Battery voltage input.
VDD_BYP_CHG	M10		VCHG	Charger input to Bypass regulator. **NOTE** If using no charger, connect VDD_BYP_CHG direct to SMPS_VCHG.
VDD_BYP	L11			Bypass regulator decoupling.
SMPS_DCPL	M11	Analog	-	Analog power pad. Either battery or charger inputs are switched into this decoupling pad.
SMPS_VBAT	M12	Supply	VBAT	Supply to SMPS power switch from battery.
SMPS_VCHG	H13		VCHG	Supply to SMPS power switch from charger input.
VDD_PADS_1	G13		-	1.8 V/3.3 V PIO supply.
VDD_PADS_2	J1			
VDD_PADS_3	M1			
VDD_PADS_4	C13			
VDD_PADS_5	M3			
VDD_PADS_6	F2			
VDD_PADS_7	D13, E13			

1.4.10 Ground device terminal functions

Table 1-12 QCC3095 VFBGA Ground device terminal functions

Ground	Ball	Description
VSS_XTAL_OSC	B3	Ground connection for crystal oscillator.
VSS_AUX	C3	Ground connection for AUX circuits.
VSS_BT	C1, C2, D2, D3, E1, E2	Ground connection for Bluetooth. For best RF performance, each group of VSS_BT pins should have individual via connections to the ground reference plane. ■ Pin C1: Internal baseband ground ■ Pin C2: LO ground point ■ Pins D2 and D3: Analog and ESD ground ■ Pins E1 and E2: RF Balun ground
VSS_DIG_PADS	F7, F8, G7, G8	Ground for digital I/Os.
VSS_PMU	K11, K12, L12	Clean ground connection for PMU circuits.
VSS_SMPS_DIG	L13	Ground pad for Digital SMPS.
VSS_SMPS_1V8	K13	Ground pad for analog SMPS.
VSS_AUDIO_HP_SPK1	A10	Ground VSS for HP/SPK1.
VSS_AUDIO_HP_SPK2	A13	Ground VSS for HP/SPK2.
VSS_AUDIO	C4, C5, C6, C7, C8	Ground for audio circuits.
VSS_AUDIO_REF	B8	Ground for audio reference.

1.5 QCC3095 VFBGA PCB design and assembly considerations

Recommendations to achieve maximum board-level reliability of the QCC3095 VFBGA integrated circuit (IC) package.

- Use of nonsolder mask defined (NSMD) lands (lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Use via-in-pad technology to achieve the best quality NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible. Take into consideration its current carrying and the radio frequency (RF) requirements.
- 35 µm thick (1 oz) copper lands are recommended rather than 17 µm thick (0.5 oz). This results in a greater standoff which provides greater reliability during thermal cycling.
- A printed circuit board (PCB) land diameter of 0.25 mm to 0.28 mm is recommended.
- Solder paste is preferred to flux during the assembly process because it adds to the final volume of solder in the joint, increasing its reliability.
- When using a nickel gold plating finish, keep the gold thickness below 0.5 µm to prevent brittle gold/tin intermetallics forming in the solder.

1.5.1 Typical solder reflow profile

For further information describing the reflow profile of an IC when attaching its physical connection solder points to a PCB see *Typical Solder Reflow Profile for Lead-free Devices Information Note* (80-CT462-1).

1.6 Moisture sensitivity level

QCC3095 VFBGA is qualified to moisture sensitivity (MSL3) in accordance with JEDEC J-STD-020.

2 Bluetooth subsystem

The Bluetooth subsystem, see Figure 2-1, is a dual-mode radio supporting concurrent classic and Bluetooth Low Energy operation.

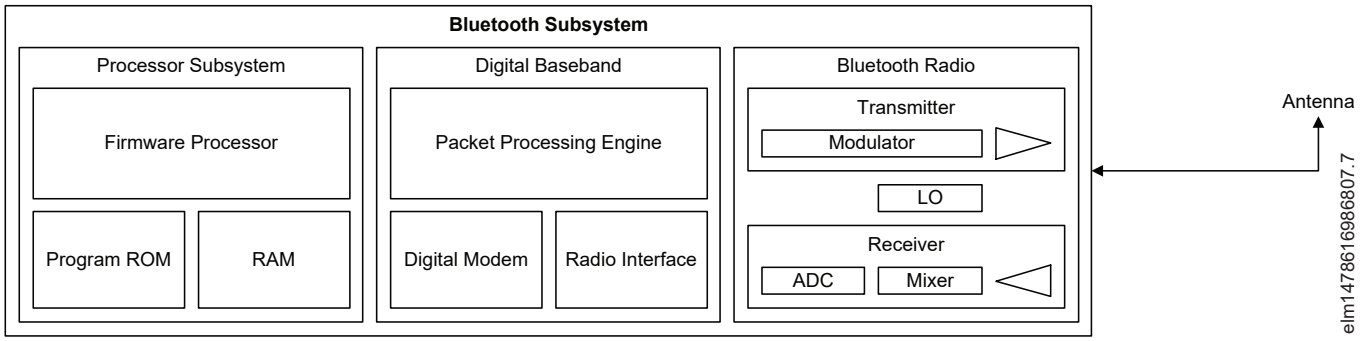


Figure 2-1 Bluetooth subsystem

The Bluetooth subsystem is fully qualified to the Bluetooth v5.4 specification. It has:

- 32 MHz/64 MHz processor running Bluetooth firmware
- Bluetooth packet processing engine and modem
- Single power domain under the control of the System Manager subsystem
- Power and clocks automatically removed to reduce power when the Bluetooth radio is not operating

NOTE For Bluetooth feature details, see ADK documentation.

2.1 Bluetooth v5.4

QCC3095 VFBGA supports Bluetooth v5.4 including Bluetooth Low Energy 2 Mbps and Bluetooth Low Energy Isochronous Channels.

2.2 Bluetooth radio

The Bluetooth radio consists of a single RF I/O port shared for receive and transmit. The RF port impedance is 50 Ω when operating.

2.2.1 Receiver

The receiver consists of an LNA that boosts the incoming RF signal. The passive mixer down-converts the wanted signal and splits the wanted output between in-phase and quadrature (IQ) related channels. Passive low pass filtering at the output of the mixer attenuates out of band signals while allowing the wanted signal to pass through. This helps to avoid saturating the ADC input.

LNA, Mixer, and ADC gains are automatically controlled by the AGC and are based on saturation detection and wideband RSSI detection indications from the RF front end.

The receive ADC is a continuous time third order sigma-delta architecture.

2.2.2 Transmitter

QCC3095 VFBGA uses a polar transmit architecture to implement the transmitter. It has separate paths for phase and amplitude modulated data:

- Basic rate modulation - uses phase modulation (PM)
- Enhanced data rate modulation (EDR2 and EDR3) - uses phase modulation and amplitude modulation

An advantage of the polar transmit architecture is that it uses a nonlinear PA. The Class-D design of the QCC3095 VFBGA PA, provides high-power efficiency in comparison to previous generations of devices.

2.3 Qualcomm Bluetooth High Speed Link

Qualcomm Bluetooth High Speed Link is a proprietary physical layer that defines:

- Robust modulation and coding schemes
- Packet structure
- Supporting protocols

Qualcomm Bluetooth High Speed Link can be used with Bluetooth Classic connections and Bluetooth Low Energy connections resulting in improved link performance or efficiency. It offers data rates from 2 to 6 Mbps that are automatically selected by an appropriate rate selection algorithm.

3 Crystal oscillator

The crystal oscillator frequency directly determines the output RF frequency and must therefore fall within the Bluetooth specification requirement of ±20 ppm maximum. This specification applies over the operating temperature and lifetime of the device.

Table 3-1 Crystal oscillator frequency accuracy

Parameter	Min	Typ	Max	Unit
Crystal oscillator frequency accuracy	-	-	±20	ppm

Capacitors are used to pull the crystal onto frequency and compensate for **initial frequency errors** (the difference between the programmed frequency and the actual oscillating frequency caused by the crystal and its PCB connections. It is also called calibration tolerance or frequency tolerance). QCC3095 VFBGA contains an array of internal capacitors, which are configured by the firmware to apply a load to XTAL_IN and XTAL_OUT.

The crystal load capacitance is adjusted using the `XtalLoadCapacitance` and `XtalFreqTrim` MIB keys. Both parameters are used to tune the frequency as precisely as possible.

Table 3-2 Typical load capacitance trim

Parameter	Min	Step size	Max	Unit
`XtalLoadCapacitance` (coarse trim)	1	0.4	13.8	pF
	0x00	0x01	0x1F	-
`XtalFreqTrim` (fine trim)	-0.5	0.025	0.5	pF
	-16	1	15	-

For more detailed information, see *QCC3095 VFBGA Hardware Design Guide* (80-74170-1).

4 System power states

Figure 4-1 shows the static QCC3095 VFBGA power states and functions available in each state. In a low-power scheme, software moves QCC3095 VFBGA between the power states to reduce total system power.

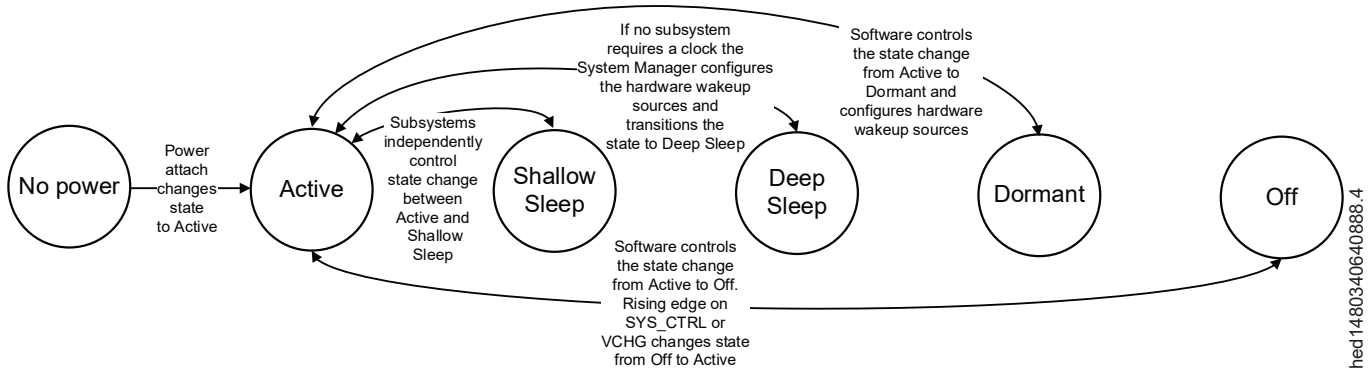


Figure 4-1 QCC3095 VFBGA static power states diagram

4.1 No Power state

When the QCC3095 VFBGA has no power, it is in the No Power state. When power is present, for example on battery attach, the QCC3095 VFBGA automatically boots and moves to the Active state.

4.2 Active state

In the Active state, the on-chip clocks and power supplies are running, and all functions of the QCC3095 VFBGA are available.

The chip operates at 0.8 V digital supply for audio sub-system clock frequencies up to 120 MHz and at 0.9 V digital supply for clock frequencies above 120 MHz and up to 240 MHz. The system manager dynamically switches the supply voltage upon request from the audio sub-system.

4.3 Shallow Sleep state

The Shallow Sleep state is functionally the same as the Active state. However, individual subsystems can independently control when they enter the Shallow Sleep state to conserve power. In the Shallow Sleep state, a subsystem can turn off or reduce the frequency of clocks and/or power down memories.

4.4 Deep Sleep state

In the Deep Sleep state, the main digital power rail (VDD_DIG_CORE) is at 0.7 V or 0.8 V digital supply. The main digital clocks are stopped and a limited number of device features remain active, including:

- Boot Manager
- LED PWM drivers

QCC3095 VFBGA uses digital power islands. The Deep Sleep state current varies significantly depending on which functions are active or in state retention.

The following events can move QCC3095 VFBGA to the Active state (selectable using software) from the Deep Sleep state:

- A rising edge on SYS_CTRL
- A rising edge or a falling edge on VCHG
- Activity on any PIO
- Activity on any digital interface
- A timer
- Digital activity on any LED pads (when configured as a digital input)
- Activity on the debug interfaces
- USB device resume

4.5 Dormant state

In the Dormant state, the PMU is enabled in an ultralow power mode. The main digital supply (VDD_DIG_CORE) is off. This configuration reduces power consumption but limits available device features.

In the Dormant state, the following inputs can transition the QCC3095 VFBGA to the Active state (selectable via software):

- A rising edge on SYS_CTRL
- A rising edge or a falling edge on VCHG
- Activity on any PIO[8:1]
- A timer

  NOTE Timer accuracy in Dormant state is limited to ±20 %
- Digital activity on any LED pad (when configured as digital inputs)

NOTE In Dormant state the 1.8 V SMPS is enabled in ULP mode and all PIO pins apart from PIO[8:1] are held in their reset state, see *Related Information*. When designing for Dormant state use, QTIL recommends minimizing leakage current from PIO pulls and external circuitry.

RELATED INFORMATION

"PIO device terminal functions" on page 24

4.6 Off state

The Off state is different to the No Power state because the QCC3095 VFBGA has power attached from VBAT. In the Off state the following events boot the chip and transition it to the Active state:

- A rising edge on SYS_CTRL per Section 15.6
- A rising edge on VCHG per Table 13-2

NOTE The device cannot power off with VCHG attached. The Dormant state is the lowest possible power state when voltage is present on the VCHG input.

4.7 Transition between static power states

Transition into the Shallow Sleep and Deep Sleep states is automatic, with the system constantly entering the lowest power mode. Transition into the Dormant and Off states is through application software control.

NOTE On transitions from No Power or Off states, all pins are in a defined state 50 ms after the transition.

4.8 Power islands

To reduce digital leakage, the Bluetooth, Audio, and Applications subsystems are contained within separate power islands. When these subsystems are enabled, power is supplied automatically.

5 Host Interfaces subsystem

In QCC3095 VFBGA all host interfaces are located together in their own subsystem called the Host Interfaces subsystem, see Figure 5-1.

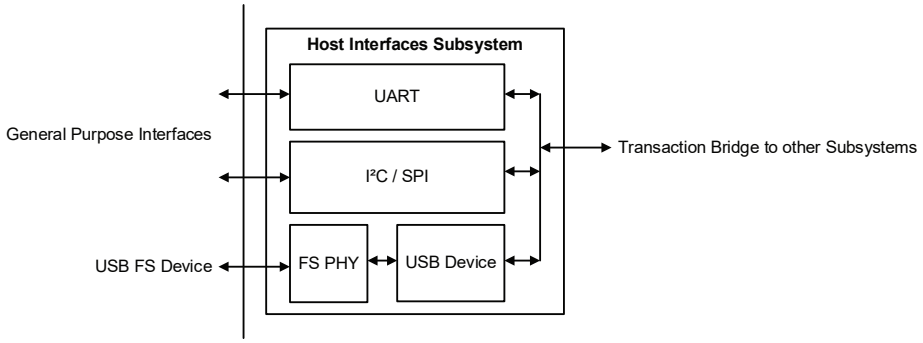


Figure 5-1 Host Interfaces subsystem

The Host Interfaces subsystem shares its host interfaces with other QCC3095 VFBGA subsystems, such as;

- Applications subsystem
- Bluetooth subsystem
- Audio subsystem, and so on

The host interfaces are shared efficiently as if each subsystem had access to a dedicated interface. Host interfaces can operate concurrently, with the System Manager allocating host interface resources to individual subsystems as required.

Each subsystem serviced by the Host Interfaces subsystem has its own memory management unit (MMU). These MMUs are accessed directly by the Host Interfaces subsystem via the transaction bus, with transaction bus interrupts routed to the correct QCC3095 VFBGA subsystem.

5.1 Host Interfaces subsystem features

QCC3095 VFBGA supports the following Host Interfaces:

- USB device
  - Full speed (12 Mbps)
  - Multiple IN and OUT endpoints, allocable individually
  - Charging support
- UART
  - Supports H4 HCI interface or raw UART to application
- 3 x bit serializers that are configurable independently as
  - I²C master
  - SPI master
- These host interfaces can operate concurrently, subject to pin multiplexing constraints, between the UART, SPI, and I²C

Host interface signals for UART, SPI, and I²C go through a PIO multiplexer, with a further multiplexing implemented at the top level to the PIOs. The Host Interface subsystem must be selected as the controlling subsystem for the relevant PIOs.

5.1.1 UART interface

QCC3095 VFBGA has a standard UART serial interface that provides a simple mechanism to communicate with other serial devices using the RS232 protocol. The UART interface multiplexes with PIOs and other functions. Hardware flow control is optional. Table 5-1 lists possible UART settings.

Table 5-1 UART configuration options

Parameter		Possible value
Baud rate	Minimum	2400 Bd (≤2%Error)
		19,200 Bd (≤1%Error)
	Maximum	4 MBd (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd, or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 5-2 lists common baud rates and the QCC3095 VFBGA baud rate percentage deviation from that rate.

Table 5-2 Standard UART baud rates

Baud rate	Baud rate error (%)
1200	18.62
2400	-1.73
4800	-1.73
9600	-1.73
19200	0.82
38400	-0.45
57600	-0.03
76800	0.18
115200	-0.03
230400	-0.03
460800	-0.03
921600	0.02
1382400	0.01
1843200	0.00
2764800	0.01
3686400	0.00
4000000	0.00

5.1.2 Bitserial operating as a SPI master

Figure 5-2 and Figure 5-3 show bitserial interface timings with different clock phase (CPHA).

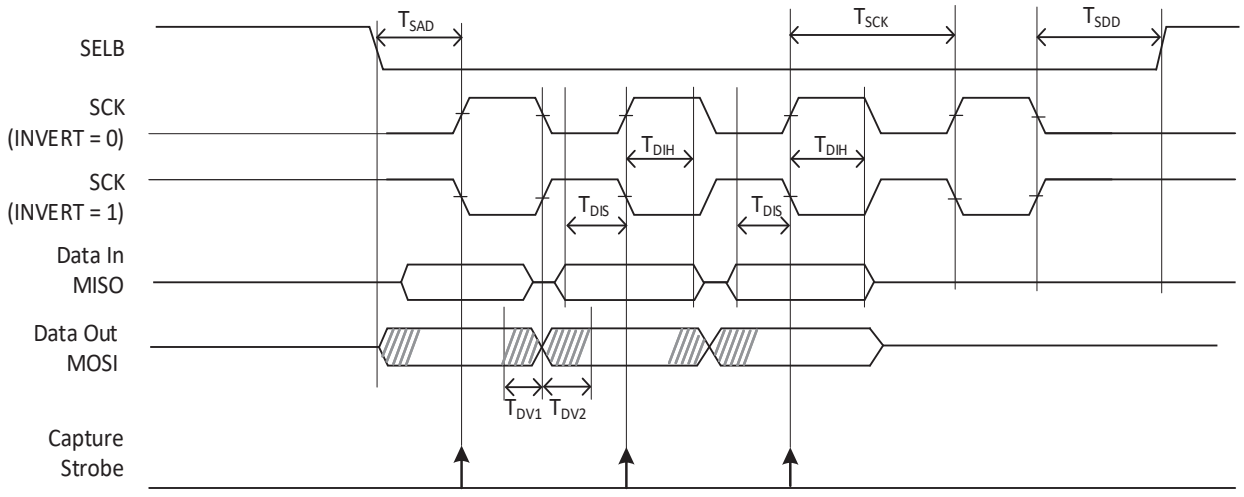


Figure 5-2 Bitserial M-SPI timing diagram, operating modes with CPHA = 0

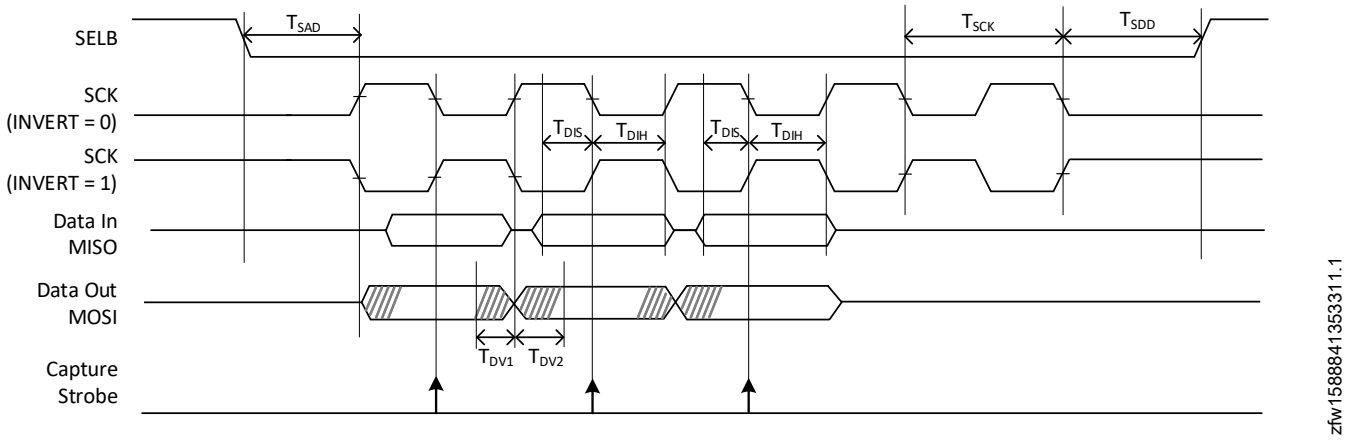


Figure 5-3 Bitserial M-SPI timing diagram, operating modes with CPHA = 1

Table 5-3 lists bitserial interface timing parameters.

Table 5-3 Bitserial M-SPI timing parameters

Parameter	Symbol	Min	Max	Unit	Notes
Clock period	T_{SCK}	125	-	ns	-
Sel Assert to SCK rise delay	T_{SAD}	17.0	-	ns	-
SCK fall to SEL de-assert delay	T_{SDD}	52.5	-	ns	-
MISO data setup	T_{DIS}	39.0	-	ns	-
MISO data hold	T_{DIH}	0.0	-	ns	-
MOSI data invalid minimum	T_{DV1}	-13.0	-	ns	Total data invalid window of 28.1 ns
MOSI data invalid maximum	T_{DV2}	-	15.1	ns	

When operating as a SPI master the Bitserial is clocked at half the crystal frequency. SCK frequencies are integer divisions of the Bitserial clock frequency with a minimum supported division of 2. With a 32 MHz crystal the possible SCK frequencies are 8 MHz, 5.33 MHz, 4 MHz and so on.

It is possible to program a sampling offset using the clock_sample_offset setting as shown in Equation 5-1. The offset granularity is limited to integer multiples of 31.25 ns and is always rounded down in the case of a non-integer multiple.

$$T_{OFFSET}(\text{ns}) = \left\lfloor \frac{T_{SCK}(ns)}{31.25 * 2} * {clock\_sample\_offset}/{65536} \right\rfloor * 31.25\text{ns}$$

Equation 5-1 Program a sampling offset using the clock_sample_offset setting

The default and recommended value is 0 which disables the offset.

5.1.3 Bitserial operating as an I²C master

QCC3095 VFBGA is compliant with the Fast-mode UM10204 I²C-bus specification.

6 Applications subsystem

The Applications subsystem, see Figure 6-1, is a processor-based subsystem that provides on-chip Bluetooth high-level protocol stack functionality and customer programmability.

It has two 32-bit processors, one for Qualcomm Technologies International, Ltd. (QTIL) firmware, and another for customer execution that features memory protection logic.

The primary nonvolatile program storage is off-chip flash memory interfaced using a high-speed QSPI interface. It is cached to provide program code and data for both processors, and file system data and any other data required for chip configuration. Support is software-dependent, see ADK release notes.

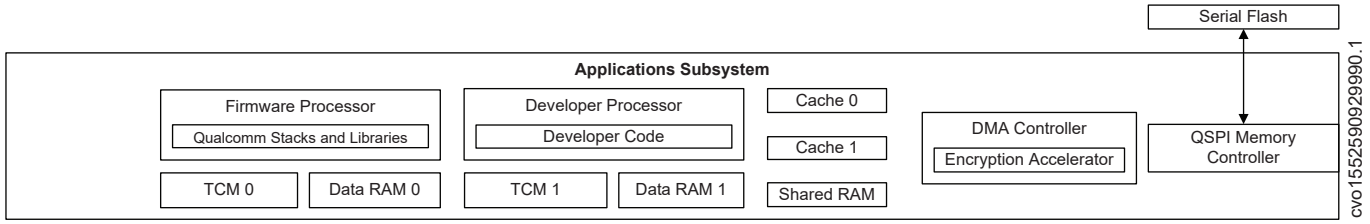


Figure 6-1 Applications subsystem

The Applications subsystem controls several peripheral interfaces such as USB device, UART, I²C, and SPI.

6.1 Application subsystem features

Application subsystem features include:

- 2 x (32 MHz or 80 MHz) central processing unit (CPU) cores using Kalimba DSP architecture:
  - 32-bit reduced instruction set computer (RISC) core with DSP features, integrated for optimal control code execution
  - Sleep mode, interrupt controller, timers, zero overhead looping
  - Private data RAM (Data RAM 1), 160 KB for Developer processor
  - 2-way cache (Cache 1) 32 KB for Developer processor
  - 128 KB of TCM (TCM 1) for Developer processor
  - Debug features such as hardware breakpoints, single step, PC trace, code instrumentation message support
- 64 KB shared buffer RAM
- A direct memory access (DMA) controller core with acceleration for data encryption and comparison, access to QSPI flash and remote subsystems
- Demand-paged buffer management hardware providing efficient use of shared memory by local and remote masters
- QSPI data path unit with support for flash at 80 MHz single data rate (SDR) using inline decryption
- Multiple remote subsystem interfaces for messaging, control, and data transfer between the various radio and audio subsystems

The Applications subsystem is powered and brought out of reset by the System Manager and starts up automatically when clocked.

The subsystem has a single power-island. Each RAM instance is controlled independently to optimize power.

6.2 QSPI Flash Controller

The QCC3095 VFBGA QSPI Flash Controller connects to external serial flash using a QSPI interface. Figure 6-2 shows timing requirements for the QCC3095 VFBGA QSPI interface.

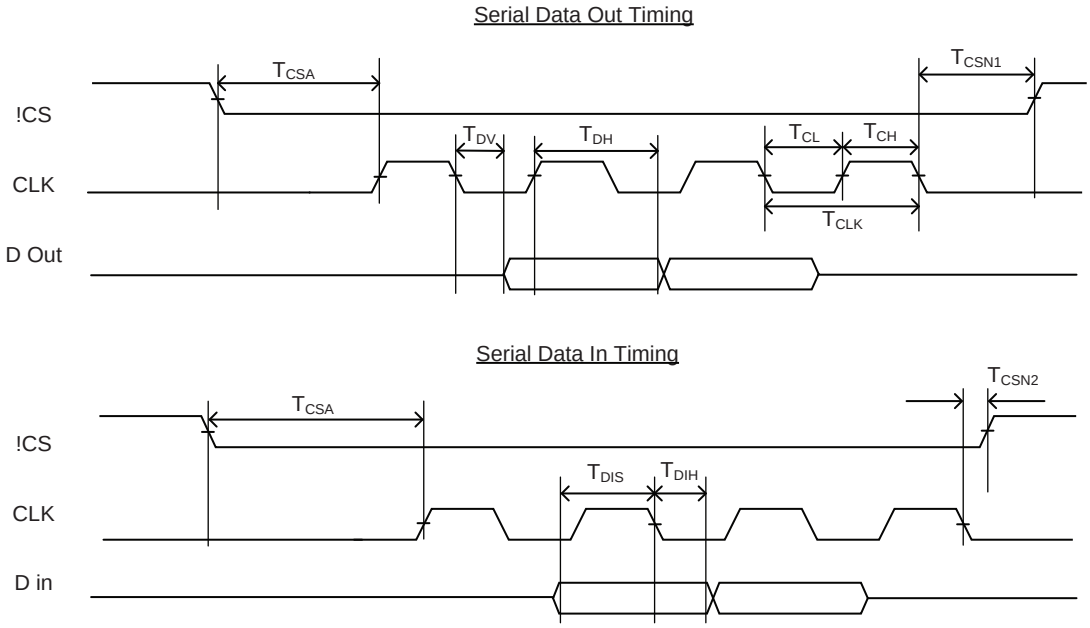


Figure 6-2 QCC3095 VFBGA QSPI interface timing

Table 6-1 and Table 6-2 list performance to be met over the operating temperature range unless otherwise stated.

Table 6-1 Timing parameters for 80 MHz SDR operation

Parameter	Min	Typ	Max	Units	Description
T_{CLK}	12.5	-	-	ns	Clock period
T_{CL}	6.0	-	-	ns	Clock Low period
T_{CH}	6.0	-	-	ns	Clock High period
T_{CSA}	-	-	19.8	ns	CS Active to Clock Active
T_{DV}	-	-	3.7	ns	Data Out Valid time
T_{DH}	3.0	-	-	ns	Data Out Hold time
T_{CSN1}	34.5	-	65.5	ns	CS Not-active Hold time (write)
T_{CSN2}	-	-	28.0	ns	CS Not-active Hold time (read)
T_{DIS}	6.3	-	-	ns	Data Input Setup time
T_{DIH}	0	-	-	ns	Data Input Hold time

Table 6-2 Timing parameters for 32 MHz SDR operation

Parameter	Min	Typ	Max	Units	Description
T_{CLK}	31.25	-	-	ns	Clock period
T_{CL}	15.0	-	-	ns	Clock Low period
T_{CH}	15.0	-	-	ns	Clock High period
T_{CSA}	-	-	57.3	ns	CS Active to Clock Active
T_{DV}	-	-	3.7	ns	Data Out Valid time
T_{DH}	3.0	-	-	ns	Data Out Hold time
T_{CSN1}	90.7	-	159.3	ns	CS Not-active Hold time (write)
T_{CSN2}	-	-	65.5	ns	CS Not-active Hold time (read)
T_{DIS}	24.0	-	-	ns	Data Input Setup time
T_{DIH}	0	-	-	ns	Data Input Hold time

NOTE For recommended QSPIs to use with QCC3095 VFBGA, refer to QCC518x and QCC308x ADK Software Data Sheet.

7 Audio subsystem

Figure 7-1 shows the QCC3095 VFBGA Audio subsystem.

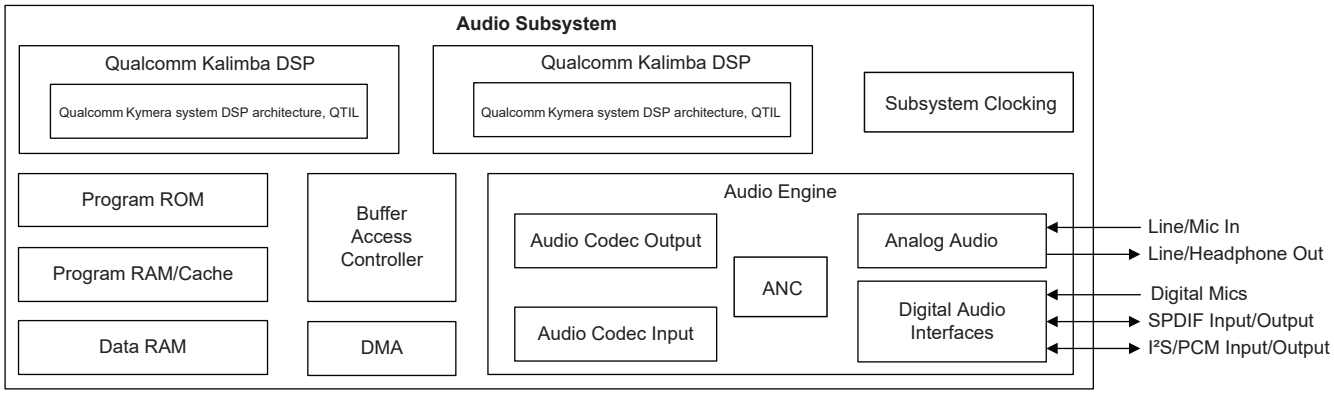


Figure 7-1 QCC3095 VFBGA Audio subsystem

7.1 Audio subsystem features

Audio subsystem features include:

- CPU clock options
  - Flexible clocking options from 2 MHz to 240 MHz for audio processing

    NOTE For details on the supported clock rates, see ADK documentation.
- Digital supply voltage
  - 0.8 V for clock frequencies up to 120 MHz
  - 0.9 V for clock above 120 MHz and up to 240 MHz
- Program RAM/cache: 384 KB
- Data RAM size: 1408 KB
- Analog DAC: Stereo analog outputs configurable as differential Class-AB audio outputs or differential high efficiency Class-D
- Analog ADC: Quad analog inputs configurable as single ended line inputs, or unbalanced, or balanced analog microphone inputs
- I²S/pulse code modulation (PCM) interface
  - 24-bit I²S interface with 1 input and 3 output channels
  - Supports 8-slot TDM
  - Supports 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz, 384 kHz sample rates
- SPDIF interfaces
  - Two instances configurable as input or output
  - Supports 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz sample rates
- Audio MCLK: Programmable, available on PIO[15]

- Audio engine
  - 2 coder decoder (codec) output channels, supporting 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, 192 kHz sample rates
  - 16 codec input channels supporting 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz sample rates
- Digital microphones
  - Five interfaces supporting up to ten microphones
  - Supports 500 kHz, 571 kHz, 666 kHz, 800 kHz, 1 MHz, 1.33 MHz, 2 MHz, and 4 MHz clock frequencies
- ANC: Hybrid, Feedforward, and Feedback modes

7.2 Dual core Kalimba

The audio subsystem has identical 2 x 32-bit, clocked up to 240 MHz dual Kalimba cores. The Kalimba cores have extended 8 x 8 and 16 x 16 multiplier and accumulator (MAC) instructions for optimal implementation of machine learning algorithms. Each core has its own set of timers, interrupt controllers, and caches. Caches are implemented in program RAM. Both Kalimba cores have identical memory maps that enable them to see all RAMs, NVM interfaces, and buffers in remote subsystems and shared peripherals, such as codec and buffer access controller.

The Kymera framework runs on the audio subsystem processors to communicate with the rest of the device.

7.3 Program ROM

The Audio subsystem has an on-chip ROM.

7.4 Program RAM and caches

The Audio subsystem has 384 KB of program RAM implemented as 48 banks of 8 KB each. Caches are implemented in Program RAM.

Access for each bank is arbitrated individually. By default, each CPU has full access to entire RAM, but access permissions can be set up at a bank level. Additionally, the implementation supports execution from data RAM.

7.5 Data RAM

The Audio subsystem has 1408 KB of DM RAM divided into 44 banks of 32 KB each. All RAM banks are equally accessible by the CPUs.

Data RAM is directly accessible to the audio engine for audio streaming and for remote access.

The Kymera framework requires a specific memory size for the enabled audio DSP core. For RAM usage details, see the relevant software release note.

7.6 Buffer access controller

The buffer access controller (BAC) enables remote subsystems to access audio buffers and data RAM. The BAC implements operations to manipulate audio buffer data to save DSP million instructions per second (MIPS). Audio engine streams data in and out of buffer RAM through the BAC.

7.7 DMA

This single-channel Direct Memory Access (DMA) block provides the ability to perform multiple data copies simultaneously between memory sources and sinks in the system. It has access to all local memories in the Audio subsystem.

7.8 Audio engine

The Audio subsystem implements 16 input and 2 output codec channels for the digital and analog audio interfaces. The subsystem also implements Active Noise Cancellation hardware.

7.8.1 Active noise cancellation

The following active noise cancellation (ANC) modes are supported using digital or analog microphones:

- Hybrid ANC
- Feedforward ANC
- Feedback ANC

8 Audio interfaces

Figure 8-1 shows a summary of QCC3095 VFBGA analog audio and microphone interfaces.

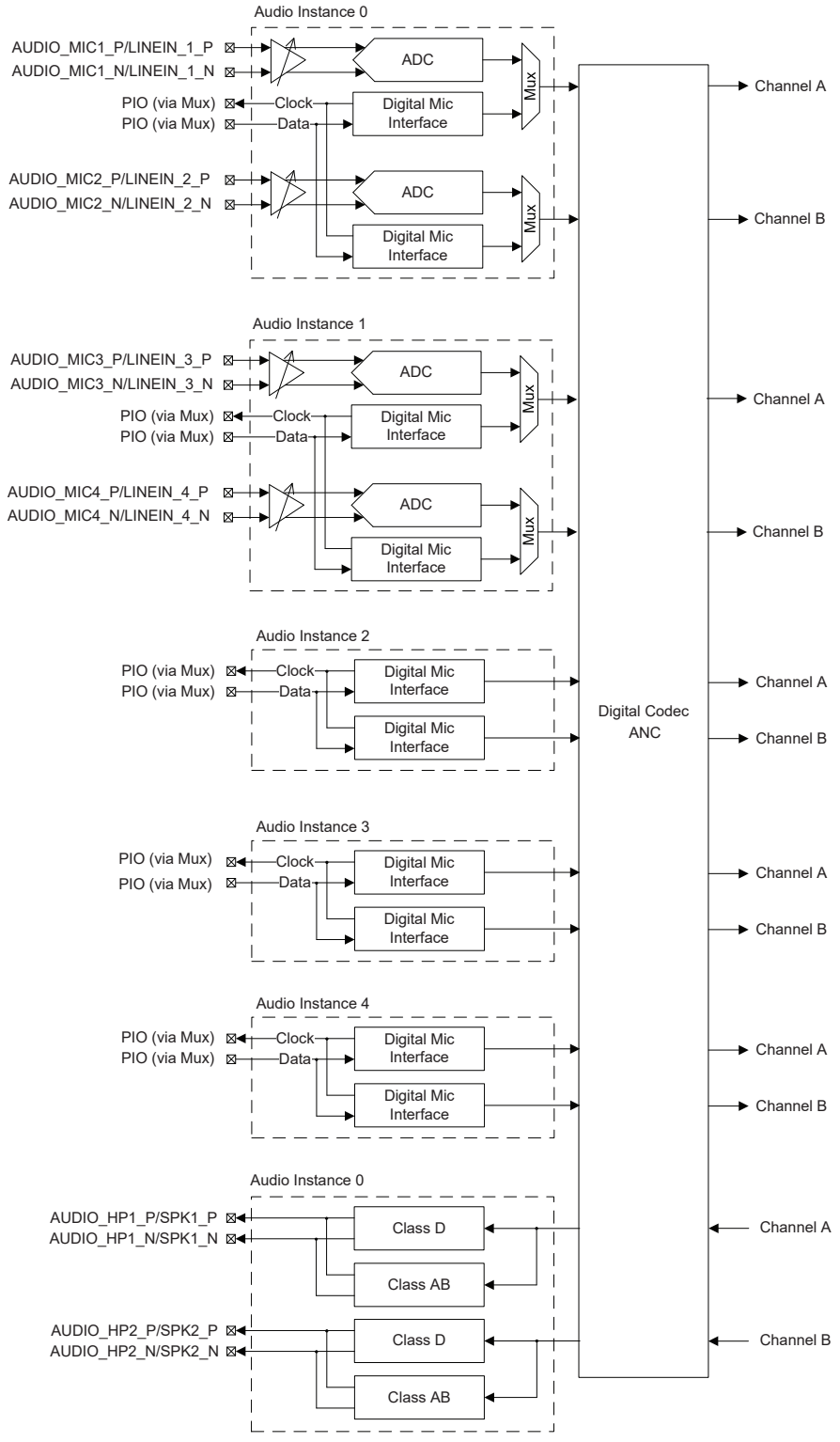


Figure 8-1 QCC3095 VFBGA analog audio and microphone interfaces

8.1 Analog audio interfaces

QCC3095 VFBGA analog audio interfaces include:

- Line/mic inputs
- Line/headphone outputs

8.1.1 Line/mic inputs

QCC3095 VFBGA has four high-quality audio input ADCs (HQADC) for line input use. They are also suitable for supporting mixed differential and single-ended applications. The ADC is 24-bit, and capable of sample rates from 8 kHz to 96 kHz. The HQADC is configurable, with an internal switch arrangement, see Figure 8-2, where VAG is a virtual ground reference. The software API allows for direct control of the nine switches, or a simpler control, supporting three standard modes:

- Stereo differential input (switch value `0xc6`)
- Stereo single-ended input, using the P inputs (switch value `0xa5`)
- Stereo single-ended input, using the N inputs (switch value `0x14a`)

Inputs should be AC coupled, typically using a 2.2 µF capacitor. Reducing this capacitor value, reduces low-frequency response attenuation.

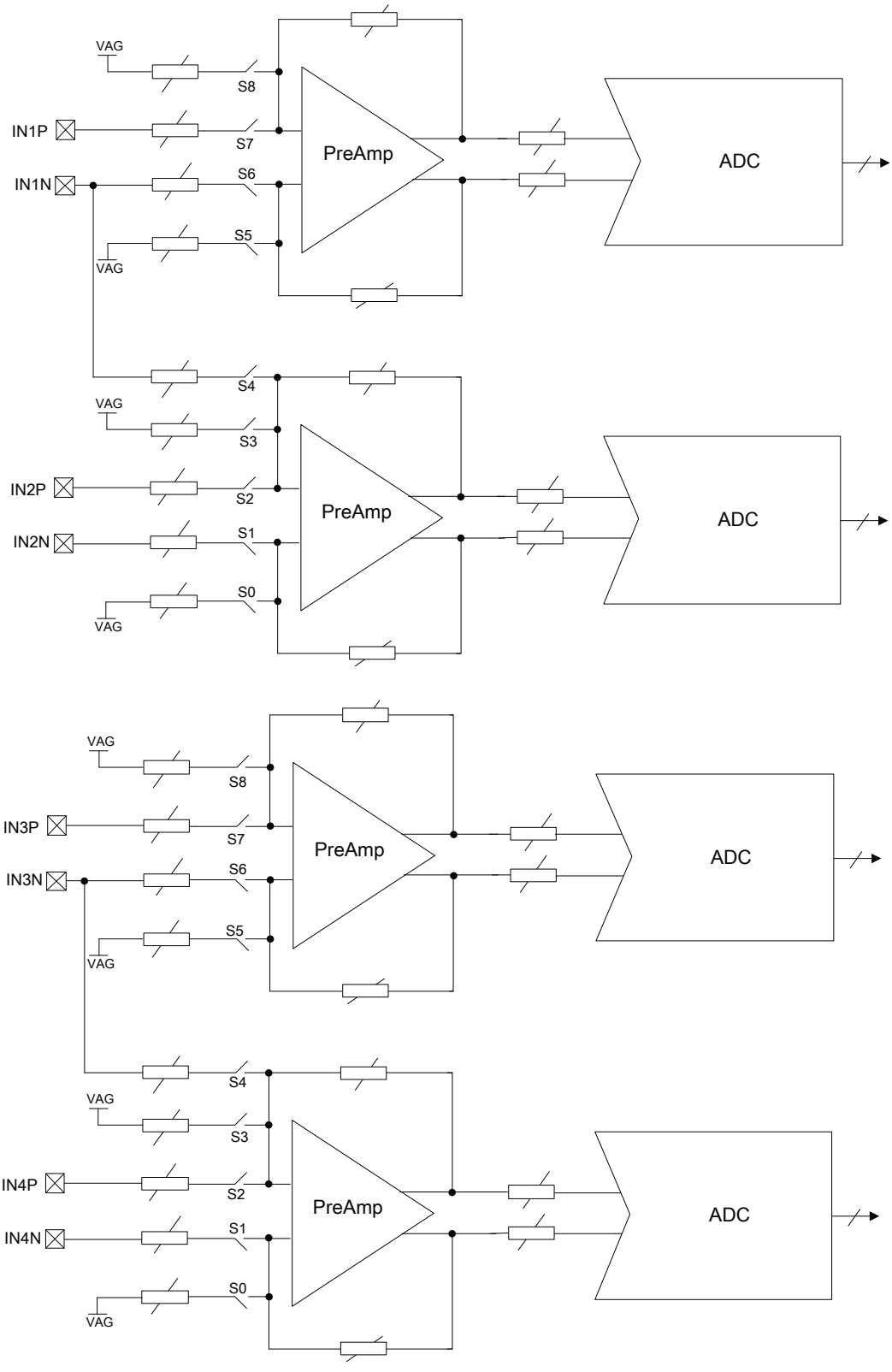


Figure 8-2 QCC3095 VFBGA high-quality ADC input switch configuration

Each ADC channel receives a differential/single-ended input and generates a 3-bit Delta-Sigma modulated output that goes into a decimator. The ADC serves both line and mic modes. Both channels have independent references, and most control signals are also independent.

The input is fed into a programmable gain amplifier. The audio output from the pre-amplifier stage is always differential and has a maximum amplitude of 2.4 Vpp (peak-to-peak). The pre-amplifier can support single ended and differential inputs at the same input amplitude. At 0 dB gain the maximum input is 2.4 Vpp, see Table 8-1.

Table 8-1 High-quality ADC analog gain vs. input impedance and input amplitude

Analog system gain (dB)	Input impedance (kΩ)	Input amplitude (mVpp, differential, and single ended)
0	20	2400
3	20	1699
6	20	1203
9	20	852
12	20	603
15	20	427
18	20	302
21	20	214
24	20	151
27	10	107
30	10	76
33	10	54
36	10	38
39	10	27

If the audio signal is single-ended, the input goes approximately 300 mV below ground and approximately 300 mV above the 1.8 V audio power supply rail. The input impedance is 20 kΩ with gains 0 dB to 24 dB, and 10 kΩ at higher gains. Use a typical gain of 0 dB for line-input. Use higher gain settings when a low-level MIC signal is sampled. The ADCs for both channels are driven with an 8 MHz clock and produce a digital output with the same rate.

The ADC clocks are derived from a 32 MHz low jitter reference clock.

QCC3095 VFBGA has a microphone bias source, capable of biasing four external analog microphones at a load current of up to 6 mA.

8.1.2 Mic bias regulator

QCC3095 VFBGA incorporates a low noise linear regulator for supplying electret or MEMS microphones, with an output voltage configurable from 1.5 V to 2.1 V and maximum output current of 6 mA.

8.1.3 Line/Headphone outputs

Two high-quality audio output DACs (HQDAC) drive stereo low impedance differential loads (bridge-tied load (BTL) headphones) or Line out.

DAC clocks are derived from a 32 MHz low jitter reference clock.

The HQ-DACs support two modes of operation. Class-D is a high efficiency, switching mode amplifier. The secondary Class-AB is a linear amplifier and consumes more power.

Table 8-2 Headset output driver modes

Mode	Description
Class-D	Enables a lower power consumption for the headset. 3-state BD modulation enables a filter-free configuration. Directly driven from the digital circuitry. Most of the analog portion is powered-down. Drives differential headphone loads of 16 Ω/32 Ω.
Class-AB	Enables either headphone or speaker applications. Can drive the same headphone outputs instead of switching to Class-D. Typically, useful for driving high impedance loads such as differential line out, or analog input power amp.[a]

[a] Additional external filtering may be required for line out applications that drive an active component such as a power amplifier. For more detailed information, see *QCC3095 VFBGA Hardware Design Guide* (80-74170-1)

8.2 Digital audio interfaces

Audio digital interfaces include:

- Digital microphone inputs
- Standard I²S/PCM interface
- SPDIF interface
- Audio MCLK

8.2.1 Digital microphone inputs

Up to ten channels of digital microphone inputs are supported. These are grouped as five pairs.

Most digital mics can be configured to enable two microphones to share a single data line. Figure 8-3 shows how QCC3095 VFBGA supports this mode by outputting data from one microphone on the rising clock edge and from the other microphone on the falling edge of the clock, while otherwise tri-stating their output.

Eight digital microphone clock frequencies can be generated. Configurable at: 500 kHz, 571 kHz, 666 kHz, 800 kHz, 1 MHz, 1.33 MHz, 2 MHz, and 4 MHz clock frequencies.

The digital microphone function can be assigned to PIOs, see *Related Information*.

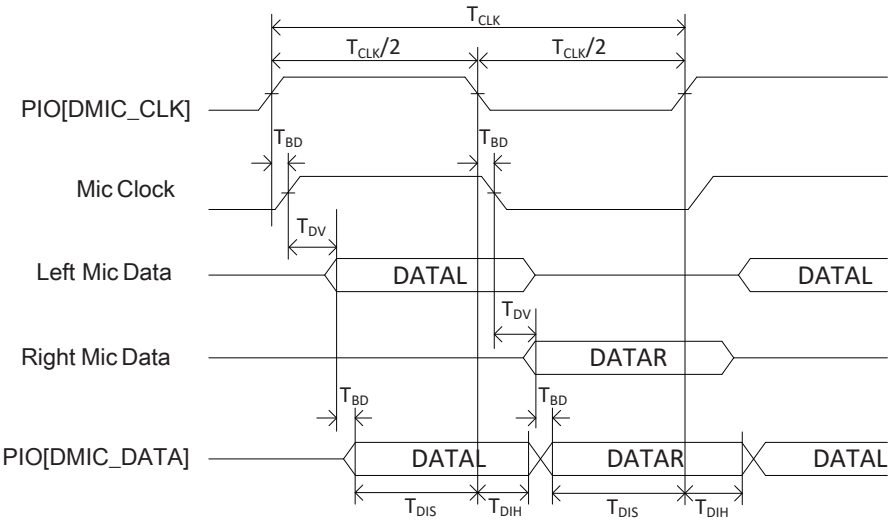


Figure 8-3 Digital microphone timing

Table 8-3 Digital microphone timing parameters

Parameter	Min	Typ	Max	Unit	Description
T_{CLK}	250	-	2000	ns	Clock period
T_{BD}	-	-	-	ns	One-way routing delay from/to QCC3095 VFBGA to/ from the digital microphone IC
T_{DV}	-	-	-	ns	Delay internal to the digital microphone from the edge of the IC clock to valid data presented by the digital microphone
T_{DIS}	40	-	-	ns	Data Input Setup time
T_{DIH}	0	-	-	ns	Data Input Hold time

RELATED INFORMATION

"PIO device terminal functions" on page 24

8.2.2 Standard I²S/PCM interface

QCC3095 VFBGA provides up to three standard I²S/PCM interfaces capable of operating up to 384 kHz sample rate.

The I²S/PCM ports are highly configurable with alternate PCM modes, and have the following options:

- SYNC edge position selectable to align with start of channel data (PCM mode), or 1 clock before start of channel data (I²S mode)
- Master (generate CLK and SYNC) or Slave (receive CLK and SYNC) (PCM/I²S)
- SYNC polarity (PCM)
- Long or short SYNC (PCM)
- Left or right justification (PCM/I²S)
- Sign extension / zero pad (PCM)
- Optional tri-state at end of word (PCM)
- Optional invert of clock (PCM/ I²S)
- 13/16/24-bit per sample (PCM/ I²S)
- Up to eight slots per frame (PCM)

For details of software support for the Audio Interface feature, see ADK documentation.

PCM and I²S pin naming varies. Table 8-4 lists frequently used signal names.

Table 8-4 PCM and I²S pin and signal names

QCC3095 VFBGA pin name	PCM signal	I²S signal	Description
PCM_DIN	PCM_DIN	I2S_DIN / SDIN / ADCDAT	Data input
PCM_DOUT	PCM_DOUT	I2S_DOUT / SDOUT / DACDAT	Data output
PCM_SYNC	PCM_SYNC	I2S_FS / WS / LRCLK	Word sync
PCM_CLK	PCM_CLK	I2S_CLK / SCK / BCLK	Bit clock

Figure 8-4 shows examples of I²S general format.

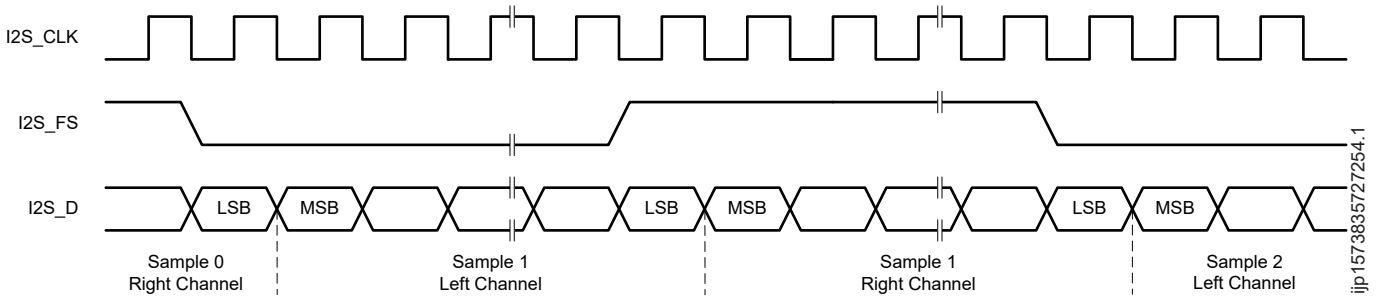


Figure 8-4 I²S general format

8.2.3 I²S/PCM master mode timing diagram

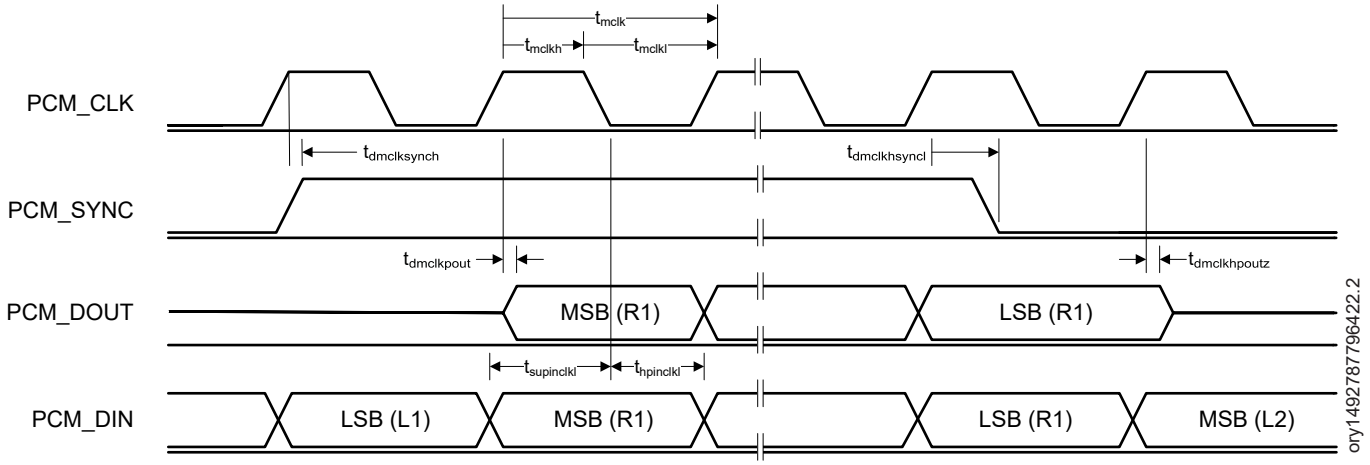


Figure 8-5 I²S/PCM master mode timing diagram

NOTE

- Diagram shows I²S standard format, but timing information also applies to PCM mode.
- PCM_DOUT to tri-state is not applicable in I²S mode, because I²S standard requires excess bits to be zero padded.
- With inverted CLK option selected the active CLK edges swap polarity.
- 1/ t_{mclk} is the audio sample frequency. I²S specification requires that t_{mclkh} and t_{mclkl} must be greater than or equal to 0.35 t_{mclk}

Table 8-5 I²S/PCM master mode timing diagram symbols

Symbol	Parameter	Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance	-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low	-	-	20	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	0	-	-	ns

8.2.4 I²S/PCM slave mode timing diagram

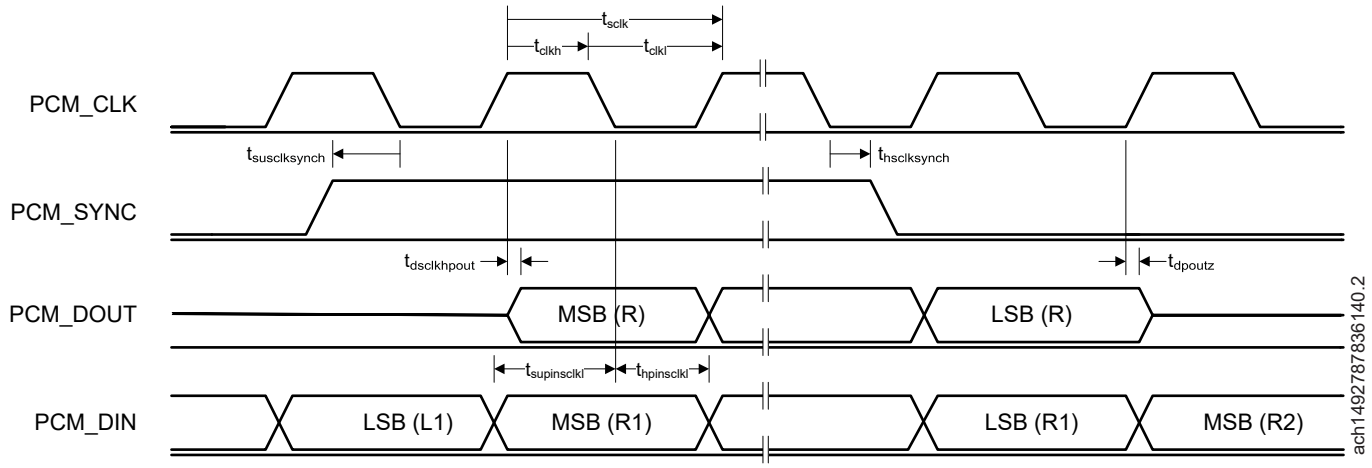


Figure 8-6 I²S/PCM slave mode timing diagram

NOTE

- Diagram shows I²S standard format, but timing information also applies to PCM mode.
- PCM_DOUT to tri-state is not applicable in I²S mode, because I²S standard requires excess bits to be zero padded.
- With inverted CLK option selected the active CLK edges swap polarity.
- 1/ t_{sclk} is the audio sample frequency. I²S specification requires that t_{sclkh} and t_{sclkl} must be greater than or equal to 0.35 t_{sclk}

Table 8-6 I²S/PCM slave mode timing diagram symbols

Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	5	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	15	-	-	ns
$t_{dsclkhpout}$	Delay time from PCM_CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_CLK high to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to PCM_CLK low	15	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	5	-	-	ns

8.2.5 SPDIF interface

SPDIF (IEC 60958) is a digital audio interface. It uses biphase coding to minimize the DC content of the transmitted signal, and enables the receiver to decode clock information from the transmitted signal. QCC3095 VFBGA has up to two SPDIF interfaces configurable as input or output. These interfaces are compatible with IEC 60958-1, IEC 60958-3, IEC 60958-4, and AES/EBU standards.

Signals are input/output via PIO and typically require external line drivers (for 75 Ω cabling) or optical transceivers (‘Toslink’). Any PIO is assignable for SPDIF use.

8.2.6 Audio MCLK

QCC3095 VFBGA has two internal clock sources for audio interfaces:

- A standard 120 MHz clock (divided down).
- An independent PLL (MPLL) that is usable as an alternate MCLK frequency clock source for the I²S/PCM and SPDIF ports.

When it cannot be generated directly from the 120 MHz clock, the MPLL can be output on a PIO for use by an external codec where low jitter I²S/PCM and SPDIF performance is required.

Table 8-7 lists the output frequencies that the MPLL can generate.

The MPLL increases system power consumption and therefore only used when necessary.

Table 8-7 Audio MCLK clock output frequencies

MCLK frequency (Hz)	Sample rate (kHz)		
	MCLK ÷ 128	MCLK ÷ 256	MCLK ÷ 384
1,024,000	8	-	-
2,048,000	16	8	-
3,074,000	24	-	8
4,096,000	32	16	-
5,644,800	44.1	-	-
6,144,000	48	24	16
8,192,000	-	32	-
9,216,000	-	-	24
11,289,600	88.2	44.1	-
12,288,000	96	48	32
16,934,400	-	-	44.1
18,432,000	-	-	48
22,579,200	176.4	88.2	-
24,576,000	192	96	-
33,868,800	-	-	88.2
36,864,000	-	-	96
45,158,400	-	176.4	-
49,152,000	384	192	-
67,737,600	-	-	176.4
73,728,000	-	-	192

8.3 Simultaneous audio routing

There are some limitations on how QCC3095 VFBGA can simultaneously use its audio inputs and outputs.

8.3.1 Audio input interfaces

Table 8-8 lists conditions in which ten input interface channels can be active simultaneously.

NOTE Each interface can only be used for an analog input or a digital microphone, but not both simultaneously.

Table 8-8 Audio input interface use conditions

Channel	Analog	Digital
Interface instance 0, Channel A	ADC 1	Digital microphone
Interface instance 0, Channel B	ADC 2	Digital microphone
Interface instance 1, Channel A	ADC 3	Digital microphone
Interface instance 1, Channel B	ADC 4	Digital microphone
Interface instance 2, Channel A	N/A	Digital microphone
Interface instance 2, Channel B	N/A	Digital microphone
Interface instance 3, Channel A	N/A	Digital microphone
Interface instance 3, Channel B	N/A	Digital microphone
Interface instance 4, Channel A	N/A	Digital microphone
Interface instance 4, Channel B	N/A	Digital microphone

8.3.2 Audio output interfaces

Table 8-9 lists conditions in which the two output channels are active simultaneously.

Table 8-9 Audio output interface use conditions

Channel	Analog
Interface instance 0, Channel A	DAC Left
Interface instance 0, Channel B	DAC Right

8.3.3 Audio slots

QCC3095 VFBGA can support a maximum of 16 active audio input slots and 8 active audio output slots simultaneously, where one slot is a single audio data stream.

Table 8-10 lists typical QCC3095 VFBGA audio slot usage.

Table 8-10 QCC3095 VFBGA audio slots

Interface	Number of slots	Notes
Stereo I²S	2	-
SPDIF	3	M, W, and user data channels per SPDIF interface
PCM	2 or 4	One slot per channel. For example, 4 channel PCM requires 4 slots
Analog ADC	4	Two per stereo ADC. For example, 2 pairs of stereo ADCs require 4 slots
Analog DAC	2	Per stereo DAC
Digital microphone	1	One slot per channel. For example, 4 digital mics require 4 slots

For example, 4 x digital microphones (4 slots) + 2 x ADC (4 slots) + 1 x Stereo I²S (2 slots) = 10 input slots.

9 Peripheral interfaces

9.1 PIO

QCC3095 VFBGA has the following digital input/output (I/O) pads:

- 53 PIO pads:
  - Including 1 x Reset (active low) pad: PIO[1]
- 6 x pads for the Applications subsystem QSPI interface
- 6 x pads intended for LED operation: LED[5:0]
- 1 x Output on standard pad: XTAL_CLKOUT
- 1 x power-on signaling: SYS_CTRL, available for use as an input after boot.

9.2 PIO pad allocation

The following QCC3095 VFBGA functions have specific pad allocations:

- QSPI (Applications subsystem)
- LED pads
- Transaction bridge
- Audio I²S/PCM

NOTE Any PIO is usable for:

- Digital microphones
- SPDIF
- UART
- Bit Serializer (I²C/SPI)
- LED PWM controllers

9.3 Standard I/O

The standard digital I/O pins (PIO) on QCC3095 VFBGA are split into separate pad domains. Each VDD_PADS domain can be separately powered, from 1.7 V to 3.6 V.

NOTE When PIOs in a supply domain are used for a high-speed interface, decoupling the respective VDD_PADS pin with a 100 nF decoupling capacitor may be beneficial. The VDD_PADS of a particular pin should be powered before voltages are applied to any PIO powered by that domain, otherwise back powering can occur through the electrostatic discharge (ESD) protection in the pad.

PIO are programmed to have a pull-up or pull down with two strengths (weak and strong). Program PIO with a sticky function where they are strongly pulled to their current input state. PIO have a reset pull state. After reset, pulls are reconfigurable using software.

PIOs also have a programmable drive strength capability with available settings of 2, 4, 8, or 12 mA. For details, see *Related Information*.

All subsystems can read all PIO. Use software to assign PIO write access to particular subsystem control. To make PIO inputs available use Schmitt triggers.

RELATED INFORMATION

"Digital terminals" on page 93

9.4 Pad multiplexing

A QCC3095 VFBGA pad function is chosen at runtime from multiple potential functions, using multiplexing.

In the input direction, signals driven into the chip, all PIOs are distributed to each subsystem and visible on the PIO status bus. The subsystem selects I/Os of interest for a particular application.

In the output direction, the System Manager has overall control of PIO allocation and control. When a PIO is allocated to a particular subsystem, the output is connected from the subsystem to the pad. There are no registers between the subsystem and the pad.

The LED pins and some other peripheral I/O states are read as virtual PIOs, see Table 9-1.

Table 9-1 Virtual PIO

Function	PIO
SYS_CTRL	PIO[0]
LED[5:0]	PIO[63:58]

9.5 RESET# reset pin

The QCC3095 VFBGA digital reset pin (RESET#) is an active low reset signal. PIO[1] defaults to RESET# on boot.

On-chip glitch filtering avoids unintended resets by filtering out spurious noise. The RESET# pin has a fixed strong pull-up to VDD_PADS_1 and can be left unconnected. The input is asynchronous, and is pulse extended within QCC3095 VFBGA to ensure a full reset.

QCC3095 VFBGA contains internal Reset Protection functionality to automatically keep the power rails enabled and enable the system to restart after an unintended reset (such as a severe ESD event). Assertion of RESET# beyond the Reset Protection timeout (typically greater than ~1.8 s) causes the device to power down if VCHG_PLUGGED is false and SYS_CTRL is low.

NOTE QCC3095 VFBGA does not power down if RESET# is asserted while VCHG_PLUGGED is true.

QTIL recommends that QCC3095 VFBGA is powered down using software-control rather than external assertion of RESET#.

Holding RESET# low continuously is not the lowest QCC3095 VFBGA power state because pull downs are enabled on VCHG and VDD_BYP in this state.

The device will be reset if RESET# held low for at least 120 µs.

After boot, PIO[1] is configurable as a digital PIO.

9.6 SYS_CTRL pin

SYS_CTRL is an input pin that acts as a power-on signal for the internal regulators. Use it as an input (virtual PIO[0] - available using software) or as a multifunction button.

From the OFF state, SYS_CTRL must be asserted for >20 ms to start power up.

SYS_CTRL is VBAT tolerant (4.8 V max), and typically connected using a button to VBAT. SYS_CTRL has no internal pull resistor, and requires an external pull-down if left undriven.

When connected using a button to VBAT a series 100 kΩ resistor should be added, see Figure 9-1. When driving SYS_CTRL from another IC the minimum series resistance required is 50 Ω.

Figure 9-1 SYS_CTRL connected to 100 kΩ resistor in series

Use software to logically disconnect SYS_CTRL from the power on signal for internal regulators. For example, when booted, software takes control of the internal regulators and the state of SYS_CTRL is ignored by the regulators.

9.7 LED

QCC3095 VFBGA has LED pads and controllers.

9.7.1 LED pads

Table 9-2 lists QCC3095 VFBGA LED pad operating modes.

Table 9-2 QCC3095 VFBGA LED pad operating modes

Mode name	Description
LED Driver	This mode drives LEDs. The pad operates as an open-drain pad, which tolerates voltages up to 6.5 V. The cathode of the LED can connect to the QCC3095 VFBGA LED pad. Each pad is rated to sink current of up to 50 mA.
Digital / Button Input	This mode is for slow input signals, typically buttons. It is not for fast switching digital inputs like SPI. For these types of inputs, use the standard PIOs. In this mode, an internal weak pull-down is enabled. Typically this mode is for active high button signals to ensure that the input returns to 0 when the button is released. The pads are 6.5 V tolerant and the logic 1 threshold is typically 1 V. In digital input mode, the logic inputs are read by the software as virtual PIO[63:58].
Analog Input	In this mode, the LED pad is an analog input port. The pad voltage routes to a 10-bit auxiliary ADC.
Disabled	This is the default state for LED pads, where the pad is 6.5 V tolerant and a high impedance with no pull-down.

9.7.2 LED controllers

QCC3095 VFBGA has six PWM-based LED controllers controlled by the Applications subsystem. Use them for driving either the LED pads (through virtual PIOs) or other available PIOs.

An application may configure the LED flash rate and ramp time using a dedicated API.

Once configured, the LED flash and ramp rate are fully hardware controlled within the LED/PWM module. It is possible to synchronize any number of the LED drivers together. Use the flash/ramp rate configuration to generate color change sequences on RGB LEDs.

LED outputs are able to operate in Deep Sleep state, but not in Dormant state.

Table 9-3 lists the LED controller pattern for QCC3095 VFBGA. Each PWM block can make use of the PIOs and LED pads (virtual PIOs).

Table 9-3 LED controller pattern

LED_PWM number	PIO									
LED_PWM[0]	-	PIO[6]	-	PIO[18]	PIO[24]	PIO[30]	PIO[36]	PIO[42]	PIO[48]	PIO[58]
LED_PWM[1]	PIO[1]	PIO[7]	-	PIO[19]	PIO[25]	PIO[31]	PIO[37]	PIO[43]	PIO[49]	PIO[59]
LED_PWM[2]	PIO[2]	PIO[8]	-	PIO[20]	PIO[26]	PIO[32]	PIO[38]	PIO[44]	PIO[50]	PIO[60]
LED_PWM[3]	PIO[3]	-	PIO[15]	PIO[21]	PIO[27]	PIO[33]	PIO[39]	PIO[45]	PIO[51]	PIO[61]
LED_PWM[4]	PIO[4]	-	PIO[16]	PIO[22]	PIO[28]	PIO[34]	PIO[40]	PIO[46]	PIO[52]	PIO[62]
LED_PWM[5]	PIO[5]	-	PIO[17]	PIO[23]	PIO[29]	PIO[35]	PIO[41]	PIO[47]	PIO[53]	PIO[63]

NOTE The configuration of the PWM controller is the same whether it drives a PIO or LED pad.

If an OEM assigns other functions, not all PIOs may be available for use with the PWM generator.

Table 9-4 shows how each LED_PWM maps to a specific virtual PIO and LED_PAD on QCC3095 VFBGA.

Table 9-4 LED_PWM to PIO to LED_PAD mapping

LED_PWM number	=	PIO number	=	LED_PAD number
LED_PWM[0]	=	PIO[58]	=	LED_PAD[0]
LED_PWM[1]	=	PIO[59]	=	LED_PAD[1]
LED_PWM[2]	=	PIO[60]	=	LED_PAD[2]
LED_PWM[3]	=	PIO[61]	=	LED_PAD[3]
LED_PWM[4]	=	PIO[62]	=	LED_PAD[4]
LED_PWM[5]	=	PIO[63]	=	LED_PAD[5]

9.8 USB

9.8.1 USB interface

QCC3095 VFBGA has a USB device interface designed for connection to a host Phone/PC or battery charging adaptor.

For details on software support for USB features, see ADK documentation.

9.8.2 USB device port

The device port is a USB2.0 Full Speed (12 Mb/s) port. Typically QCC3095 VFBGA enumerates as a compound device with a hub. The enabled audio source / sink / HID / mass storage device appears behind that hub.

The DP 1.5 k pull-up is integrated in QCC3095 VFBGA. No series resistors are required on the USB data lines.

The VCHG input of QCC3095 VFBGA is tolerant of a constant 6.5 V and transients up to 7.0 V. Use an external clamping protection device if extra overvoltage protection is required.

9.8.3 USB charger detection

QCC3095 VFBGA supports charger detection to the USB BC 1.2 specification.

It provides Data Contact Detection (DCD) using an internal current source, and provides:

- Detection of Standard Downstream Ports (SDP)
- Charging Downstream Ports (CDP)
- Dedicated Downstream Ports (DCP)

The 10-bit auxiliary ADC reads the voltage on the USB data lines. This enables detection of proprietary chargers that bias the voltage on the USB data lines.

For USB Type-C® connectors, use the LED pins to detect the voltage on the USB Configuration Channel (CC) line pins (CC1 and CC2) to detect the charge current capabilities of the upstream device.

10 Transaction bridge

The transaction bridge is an external bridge into the internal transaction bus between QCC3095 VFBGA subsystems. It is the primary debug interface and can also be used for production programming.

A USB to transaction bridge interface (TRBI200) is available. For details, contact qcsales@qti.qualcomm.com.

The transaction bridge is multiplexed on PIO[8:2], see Table 10-1.

NOTE Use a direct USB2.0 connection from a host computer to the QCC3095 VFBGA for most debugging and programming activities. For more details, see the ADK documentation.

Use USB3.0 with TRBI200 for maximum data rate.

NOTE USB3.0 signals can generate noise in the Bluetooth ISM band. For applications where sensitive RF measurements take place, QTIL recommends connecting TRBI200 using USB2.0.

The transaction bridge is a multilane interface, and only requires three wires for its minimum configuration (suitable for production programming).

NOTE The TRBI200 USB transaction bridge interface requires power for input/output buffers to be supplied externally. This voltage must match the power supply domain used for the TRB pads (VDD_PADS_1).

Minimum configuration is sufficient for production programming and code download but not for extensive debug and code tracing. The configuration in use is automatically detected.

Table 10-1 Transaction bridge PIO multiplex

TRB	PIO	Required for minimum configuration	Intermediate configuration	Full bus width
TBR_CLK	PIO[8]	Yes	Yes	Yes
TBR_MISO[0]	PIO[7]	Yes	Yes	Yes
TBR_MOSI[0]	PIO[6]	Yes	Yes	Yes
TBR_MISO[1]	PIO[5]	No	Yes	Yes
TBR_MOSI[1]	PIO[4]	No	Yes	Yes
TBR_MISO[2]	PIO[3]	No	No	Yes
TBR_MISO[3]	PIO[2]	No	No	Yes

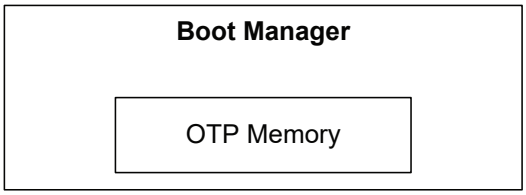
NOTE PIO[7] should not be held low during boot.

Transaction bridge debug access is lockable. When locked, this interface only becomes active after the correct unlock key sequence is provided. For more details, see the ADK documentation.

When using the transaction bridge interface, it is recommended to add an external pull-up resistor ranging 4.7 kΩ to 100 kΩ from the TRB_MISO pin to VDD_PADS.

11 Boot Manager

Figure 11-1 shows the Boot Manager.



wcn1480340633806.5

Figure 11-1 Boot Manager

The Boot Manager:

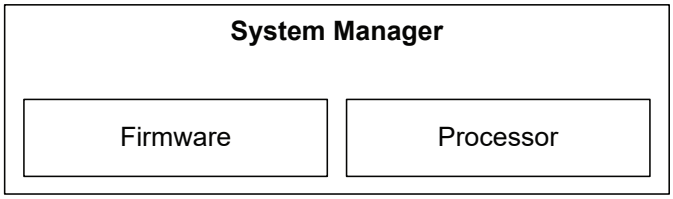
- Performs all low-level housekeeping functions
- Manages chip boot
- Manages the lowest level stages of Deep Sleep and Dormant state entry/exit

11.1 OTP memory

QCC3095 VFBGA contains one-time programmable memory areas, used to hold a customer programmable security key.

12 System Manager

Figure 12-1 shows the System Manager.



mth1478625942759.5

Figure 12-1 System Manager

The System Manager:

- Executes from ROM
- Controls the allocation of the resources in the system
- Coordinates firmware operation using message-passing and interaction with the other subsystems

Chip-level sleep modes are coordinated by the System Manager. Each subsystem indicates to the System Manager that they are asleep. The System Manager can individually disable clocks and/or power to subsystems in turn to minimize device power.

12.1 System timer

The System Manager maintains a 1 MHz system timer, which is distributed to the subsystems in the hardware using the transaction bus. The system time has 20 ppm, 250 ppm, and 20% modes to optimize current in low-power states.

13 Charging system

13.1 Li-ion charger overview and configurations

The QCC3095 VFBGA integrated Li-ion charger is designed to support single Li-ion cells with a wide range of cell capacities and variable V_{FLOAT} voltages.

It has two circuit configurations with different charge current capabilities:

- Internal configuration: Supports charge rates of 2 mA to 200 mA with no additional external components required.
- External configuration: Supports fast charge rates of 200 mA to 1800 mA with the addition of one PNP pass device and external resistor. Lower trickle and pre-charge charge currents are still available in external configuration, by switching to use the internal charge path.

Operating configuration is set in application software
using CHARGER_USE_EXTERNAL_RESISTOR_FOR_FAST_CHARGE parameter and setting the sense resistor value used.

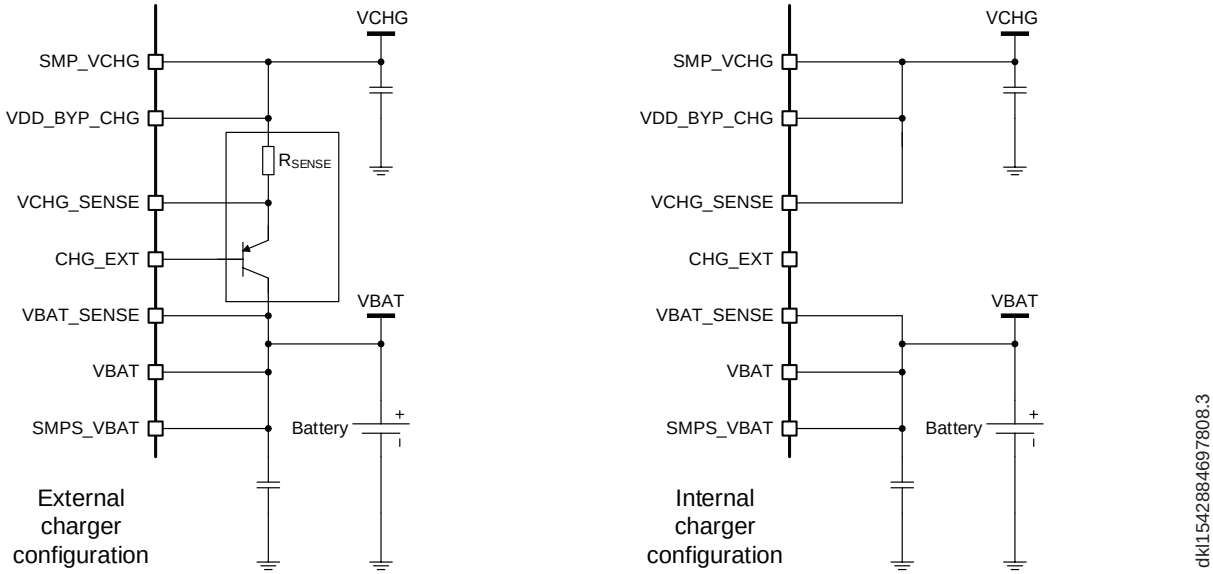


Figure 13-1 Internal and external Li-ion charger configurations

13.1.1 Charger connections

In both charger configurations, charge current enters through the VDD_BYP_CHG pin, which should be locally decoupled with a 2.2 µF ceramic capacitor.

The charger output current exits via the VBAT pin to the battery. VBAT should be locally decoupled with the C_VBAT as described in Table 13-1. C_VBAT is different between internal and external configurations. Table 13-1 shows the required VBAT net capacitance.

Table 13-1 VBAT net (C_VBAT) capacitance specification

Configuration	Min	Typ	Max	Unit
Internal	1.0 [a]	2.2	500	µF
External	1.2 [a]	4.7	500	µF

[a] Selected components must meet or exceed the minimum capacitance required including manufacturer component tolerance and voltage derate at V_{FLOAT}.

The VBAT_SENSE pin is used to sense the voltage on the battery. To avoid the IR drop in the battery PCB traces from affecting the charge process, which can lead to early termination, the VBAT_SENSE pin must be routed as a Kelvin connection (separately) to the battery connector.

Internal configuration connections

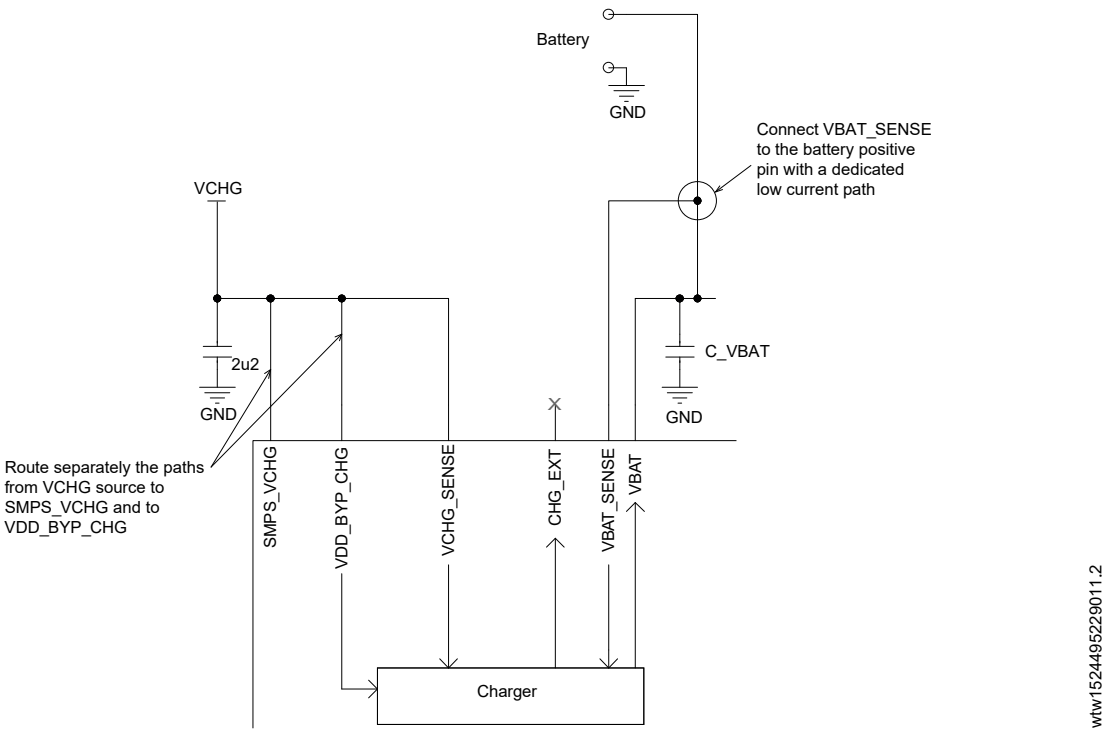


Figure 13-2 Schematic of internal charger configuration

For the internal configuration, connect the VCHG_SENSE pin to VCHG and leave CHG_EXT unconnected as shown in Figure 13-2. The charge current passes through QCC3095 VFBGA internally in all charging phases.

External configuration connections

The external configuration is used for charge currents up to 1.8 A and requires an external PNP pass transistor as shown in Figure 13-3.

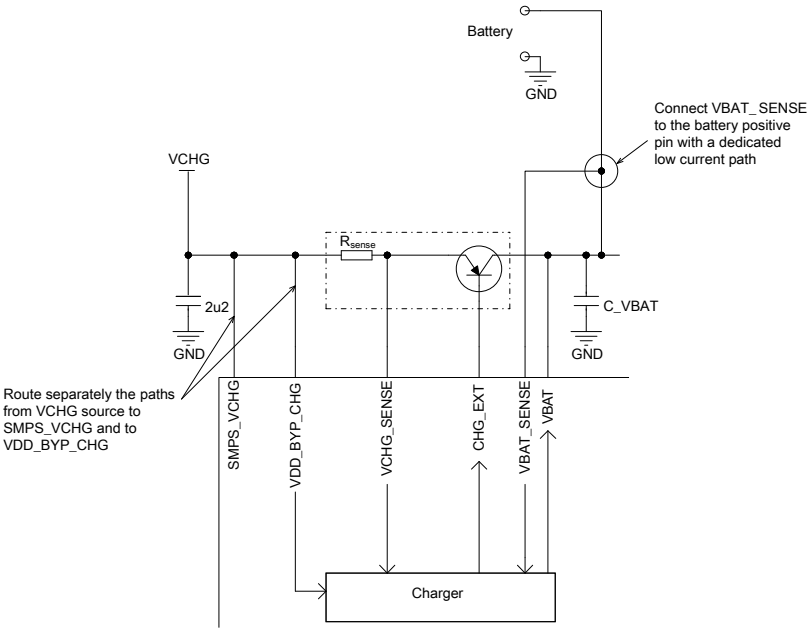


Figure 13-3 Schematic of external charger configuration

In this configuration, QCC3095 VFBGA monitors and controls the charge current using a sense resistor R_{sense} and the CHG_EXT pin.

The PNP transistor sinks current into the CHG_EXT pin so it can control the charge current. The base current of the pass transistor during normal operation is low (typically 0-3 mA depending on the pass transistor). However, if the available headroom of the charger (VCHG-VBAT) becomes small, the base current can rise significantly forcing the transistor towards saturation. As this additional base current passes through the sense resistor, it translates into a small reduction in effective charge current into the battery when the headroom is limited.

Because of the higher charge currents in the external configuration, the PCB layout can become critical and can affect charger performance. For more details, see *QCC3095 VFBGA Hardware Design Guide* (80-74170-1).

13.2 Charger input pin specification

The charger circuit accepts power input from the VDD_BYP_CHG pin. This is often referred to as the VCHG input and is connected to the VCHG inputs of other regulators. All VCHG pins (including VCHG_SENSE) share a common specification.

Table 13-2 VCHG pin specification

VCHG	Min	Typ	Max	Unit
Operating voltage (full charger specification)	4.75	5.00	5.50[a]	V
Operating voltage (reduced charger specification)[b]	4.00	5.00	5.50[a]	V
VCHG_PRESENT rising threshold	3.4	3.6	4.0	V
VCHG_PRESENT hysteresis	30	-	115	mV
VCHG_PLUGGED rising threshold	2.4	2.9	3.3	V
VCHG_PLUGGED hysteresis	100	-	600	mV

Table 13-2 VCHG pin specification (cont.)

VCHG	Min	Typ	Max	Unit
Full operating range[a]	VCHG_PRESENT	-	6.50	V
On chip pull-down (disabled when VCHG_PRESENT = 1, configurable by MIB key)	10	20	30	kΩ
Hold time to transition from Off to Active state	-	20	32	ms

[a] The VCHG pin is tolerant of voltages up to 6.5 V, but the standard specified operating range of the charger is up to 5.5 V. With VCHG at 6.5 V, the typical battery charge current will be approximately 5% greater than at 5.5 V.
[b] For details on how VCHG to VBAT headroom affects charger operation, see *Related Information*.

The VCHG_SENSE pin shares the same operating voltage specifications.

Connection and disconnection of VCHG is reported to application software and the VCHG state is also available as a virtual PIO to application software. VCHG has an internal pull down to aid compliance with USB specifications by discharging the VCHG (USB VBUS) net.

A rising voltage on VCHG passing the VCHG_PLUGGED voltage will wake the QCC3095 VFBGA from low power states (dormant and deep sleep). A rising voltage on VCHG passing the VCHG_PRESENT voltage will wake the QCC3095 VFBGA from the OFF power state.

Related Information

"Charger headroom regions and errors" on page 83

13.3 Battery pin specification

The charger outputs charge current into the VBAT pin and is connected to the VBAT inputs of other regulators. All VBAT pins share a common specification.

Table 13-3 VBAT pin specification

VBAT	Min	Typ	Max	Unit
Operating voltage	2.8	3.7	4.6	V
Boot voltage	3.0	-	4.6	V
Software power-off threshold (configurable in application)	-	3.0	-	V
USB dead/weak battery rising threshold	3.14	3.30	3.46	V
USB dead/weak battery hysteresis	50	-	120	mV

The VBAT_SENSE pin shares the same operating voltage specifications. It is used to sense the voltage on the battery and should be routed as a Kelvin connection (separately) to the battery connector. This Kelvin connection avoids the IR drop in the battery PCB traces from affecting the charger.

13.4 Charger temperature range

Unless otherwise specified, parameters are specified within the charger ambient operating temperature range listed in Table 13-4. Typically, lithium-ion cells only support charging over a limited temperature range. The charger can operate outside the range listed in Table 13-4, but performance may be degraded.

Table 13-4 Charger temperature range

Parameter	Min	Typ	Max	Unit
Charger ambient operating temperature range	-10	25	85	°C

13.4.1 Temperature measurement during charging

QCC3095 VFBGA supports use of a negative temperature coefficient (NTC) thermistor mounted near or in the cell to monitor the battery temperature. The die temperature measured in the devices PMU containing the charger is also available.

This information can be used by the application to disable charging or alter the charge current and float voltage over a range of temperatures.

Table 13-5 lists example temperature regions and behaviors depending on battery temperature range. These settings are configurable in the customer application.

Table 13-5 Example temperature regions and behaviors

Battery temperature region	Behavior
Below -10°C	Do not charge battery.
-10°C - +10°C	Charge with current and voltages suitable for low temperature conditions.
10°C - 45°C	Charge with current and voltages suitable for ambient temperature conditions.
45°C - 60°C	Charge with current and voltages suitable for high temperature conditions.
Above 60°C	Do not charge battery.

Table 13-6 Internal temperature sensor accuracy

Measurement	Min	Typ	Max	Unit
PMU temperature sensor measurement accuracy	-	-	± 5	°C

See *QCC3095 VFBGA Hardware Design Guide* (80-74170-1) for details on suitable circuits, and the ADK release documentation on how to set up the temperature controls.

13.5 General charger operation

The charger system has five charging phases, common to both internal and external configurations:

- Trickle charge
- Pre-charge
- Fast charge - Constant current
- Fast charge - Constant voltage
- Standby

Figure 13-4 shows the five phases in the charge cycle.

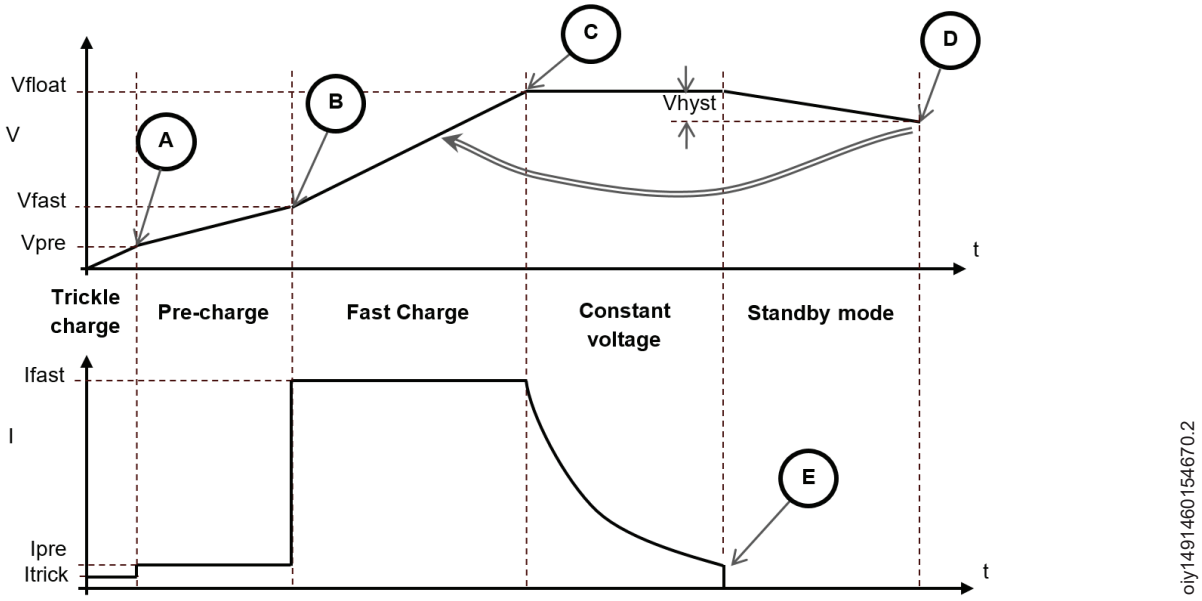


Figure 13-4 Charge cycle phases

13.5.1 Trickle charge

Trickle charge phase is entered when VBAT is sensed in the range 0 to V_{PRE}. This is encountered only with a deeply discharged battery (below V_{PRE} threshold, point (A)), or when the cell battery protection circuit has opened, temporarily disconnecting the cell.

Trickle charge phase passes a small charging current to safely charge a cell, and causes the cell battery protection circuit to reset if required. For a suitable charge current of this charging phase, see the battery manufacturers Data Sheet.

The hysteresis on the Trickle charge into Pre-charge point V_{PRE} (A) is typically 100 mV.

During Trickle charge, QCC3095 VFBGA controls charge current internally. The external pass transistor is not used.

Table 13-7 Parameters in Trickle charge phase

Trickle charge phase	Description	Min	Typ	Max	Unit
V_{PRE} threshold (rising)	Voltage at which the charger transitions out of Trickle charge into Pre-charge.	2.0	2.1	2.2	V
V_{PRE} threshold (falling)	Voltage at which the charger transitions out of Pre-charge back into Trickle.	1.9	2.0	2.1	V
I_{TRICK} (CHARGER_TRICKLE_CURRENT) NORMAL_HEADROOM region VBAT: 0 V to V_{PRE}	Trickle charge current.	2	-	30	mA
I_{TRICK} charge current accuracy over 26-30 mA range VCHG: 4.75 V to 5.5 V VBAT: 0 V to V_{PRE} I_{TRICK}: 26-30 mA NORMAL_HEADROOM region Temperature: -10°C to +85°C		-10	-	10	%
I_{TRICK} charge current accuracy over 2-25 mA range VCHG: 4.75 V to 5.5 V VBAT: 0 V to V_{PRE} I_{TRICK}: 2-25 mA NORMAL_HEADROOM region Temperature: -10°C to +85°C		-1.5	-	+2.5	mA

13.5.2 Pre-charge

Pre-charge phase is entered when VBAT is sensed in the range V_{PRE} to V_{FAST}.

The V_{FAST} threshold, point (B) (CHARGER_PRE_FAST_THRESHOLD) where the charger moves to the Fast charge phase is configurable. The hysteresis on the V_{FAST} transition from Pre-charge to Fast charge is typically 200 mV.

Charge current accuracy specification in the Pre-charge phase is the same as that in the Fast charge phase.

During Pre-charge, QCC3095 VFBGA controls the charge current internally and the external pass transistor is not used.

For a suitable charge current of this charging phase, see the battery manufacturers Data Sheet.

Table 13-8 Parameters in Pre-charge phase

Pre-charge phase	Description	Setting	Min	Typ	Max	Unit
V_{FAST} threshold (B) (CHARGER_PRE_FAST_THRESHOLD)	Voltage at which the charger transitions from Pre-charge to Fast charge.	2900	2.8	2.9	3.0	V
		3000	2.9	3.0	3.1	V
		3100	3.0	3.1	3.2	V
		2500	2.4	2.5	2.6	V
I_{PRE} (CHARGER_PRE_CURRENT) NORMAL_HEADROOM region VBAT: V_{PRE} to V_{FAST}	Pre-charge current.	-	2	-	200	mA
V_{FAST} threshold (falling) hysteresis	Hysteresis on V_{FAST} threshold (B)	-	150	200	250	mV
I_{PRE} charge current accuracy over 26-200 mA range VCHG: 4.75 V to 5.5 V VBAT: V_{PRE} to V_{FAST} NORMAL_HEADROOM region Temperature: -10°C to +85°C			-10		+10	%
I_{PRE} charge current accuracy over 2-25 mA range VCHG: 4.75 V to 5.5 V VBAT: V_{PRE} to V_{FAST} NORMAL_HEADROOM region Temperature: -10°C to +85°C			-1.5		+2.5	mA

13.5.3 Fast charge

Fast charge phase has two sub-phases:

- **Fast charge (Constant current - CC) phase**: Entered when VBAT is sensed in the range V_{FAST} to the V_{FLOAT} point (C). This is the maximum charge rate I_{FAST}, normally referred to as the fast charge current.
- **Fast charge (Constant voltage - CV) phase**: When V_{FLOAT} is reached, the cell voltage is maintained at V_{FLOAT}. The charge current slowly reduces to a percentage of the I_{FAST} value. This percentage point is configurable using CHARGER_ITERM_CTRL. At this final termination point (E) charging ends, and the charger transitions to Standby. The current termination point (E) can be adversely influenced by dynamic changes in VBAT load current, or changes in VCHG voltage.

The V_{FLOAT} voltage (C) can be configured using CHARGER_TERM_VOLTAGE from 3.65 V to 4.40 V in 50 mV increments. This enables use of cells with different V_{FLOAT} values, or cell life extension by reducing V_{FLOAT}. V_{FLOAT} can also be reconfigured depending on cell temperature if required.

Table 13-9 Parameters in Fast charge phase (Internal configuration)

Fast charge phase (Internal configuration)	Min	Typ	Max	Unit
I_{FAST} Fast charge current range (CHARGER_FAST_CURRENT) NORMAL_HEADROOM region	10	-	200	mA
I_{FAST} charge current accuracy over 26-200 mA range VCHG: 4.75 V to 5.5 V VBAT: V_{FAST} to V_{FLOAT} NORMAL_HEADROOM region Temperature: -10°C to +85°C	-10		+10	%
I_{FAST} charge current accuracy over 10-25 mA range VCHG: 4.75 V to 5.5 V VBAT: V_{FAST} to V_{FLOAT} NORMAL_HEADROOM region Temperature: -10°C to +85°C	-1.5		+2.5	mA
I_{FAST} charge accuracy (Low VCHG headroom) VBAT: V_{FAST} to V_{FLOAT} REDUCED_HEADROOM region with VCHG-VBAT > 150 mV	-40		+10	%

Fast charge phase (Internal configuration)	Min	Typ	Max	Unit
V_{FLOAT} Battery Voltage VCHG: 5 V, V_{FLOAT} of 4.20 V Temperature: 25°C	-0.5%		+0.5%	%
V_{FLOAT} Battery Voltage NORMAL_HEADROOM and REDUCED_HEADROOM regions V_{FLOAT} of 3.65 V to 4.40 V	-1%		+1%	%

Application software can be used to enable multiple ranges of I_{FAST} dependent on parameters like battery voltage and/or temperature by reconfiguring the charger as required.

Termination point (E)

The Termination point is configurable as a percentage of the configured fast charge current (I_{FAST}) and set by the parameter CHARGER_ITERM_CTRL. Three options are selectable, giving typical termination points of 13%, 24%, or 35%.

Table 13-10 lists the requested termination and typical values for various charge I_{FAST} currents at room and ambient temperatures in internal configuration. For details on software support, see ADK Software Data Sheet.

Table 13-10 Requested termination and I_{FAST} typical values in internal configuration

Requested termination (% of actual I_{FAST})	$I_{FAST\ (mA)}$	Temperature (°C)	Min (%)	Typ (%)	Max (%)
13	10 to 40	25	2	13	28
		-10 to 60	1		33
		-10 to 85	1		38
	41 to 200	25	3	13	21
		-10 to 60	1		24
		-10 to 85	1		26
24	10 to 40	25	10	24	39
		-10 to 60	3		43
		-10 to 85	3		47
	41 to 200	25	15	24	31
		-10 to 60	10		33
		-10 to 85	10		35
35	10 to 40	25	21	35	48
		-10 to 60	15		51
		-10 to 85	15		55
	41 to 200	25	20	35	39
		-10 to 60	18		42
		-10 to 85	18		44

During the CV phase of charging, the instantaneous I_{BAT} value can vary slightly as the charger loop maintains V_{FLOAT}. I_{BAT} is calculated as a moving average over 9 seconds.

If charging is started when the battery voltage is already at V_{FLOAT}, the final charger termination notification can be delayed by 8 to 10 seconds. The charger will continue to maintain V_{FLOAT} correctly throughout but charge current will continue to flow during this period. As this period is time limited, it will not adversely affect the battery.

NOTE Case communications occurring in this period can further extend the delay period as measurements are skipped in time of pause in charging during communications.

Table 13-11 Parameters in Fast charge phase (External configuration)

Fast charge phase (External configuration)		Min	Typ	Max	Unit
V_{FLOAT} Battery Voltage VCHG: 5 V, V_{FLOAT} of 4.20 V Temperature: 25°C		(-0.5%)	4.20	(0.5%)	V
V_{FLOAT} Battery Voltage V_{FLOAT} of 3.65 V to 4.40 V NORMAL_HEADROOM and REDUCED_HEADROOM regions		(-1%)	4.20	(1%)	V
Termination current	**Setting**	**Min**	**Typ**	**Max**	**Unit**
Termination current accuracy: expressed as a percentage of the actual fast charge current (I_{FAST}) obtained in the CC phase of fast charge. Temperature at 25°C, 100 mV across the sense resistor.	13 (1)	8	13	18	%
	24 (2)	19	24	29	%
	35 (3)	30	35	40	%

External configuration pass transistor	Min	Typ	Max	Unit
External pass device h_{fe}	45	120	700	-

13.5.4 Standby

The system enters Standby when the charge current has fallen below the termination current (E) and the charger terminates. In Standby, no charge current flows but the charger continues to monitor the battery voltage. If the voltage falls back below V_{FLOAT} by more than V_{HYST} (point (D)), then the charger re-enters Fast charge phase. V_{HYST} is configurable using CHARGER_STANDBY_FAST_HYSTERESIS and is expressed as a percentage of the V_{FLOAT} value.

This enables the charger system to maintain the cell near full charge while prolonging cell life.

In standby the charger continues to monitor VBAT, and therefore continues to draw some current from VCHG (up to 6 mA). To minimize system power consumption the customer application can choose to disable the charger, monitor VBAT periodically, and re-enable charging when desired.

Table 13-12 Parameters in Standby phase

Standby phase	Description	Setting	Min	Typ	Typ for V_{FLOAT} = 4.2 V (for indication)	Max
V_{HYST} threshold (D) (CHARGER_STANDBY_FAST_HYSTERESIS)	Percentage of V_{FLOAT} at which the charger transitions from Standby back to Fast charge.	100	1.8%	2.4%	100 mV	3.0%
		150	3.0%	3.6%	150 mV	4.2%
		200	4.2%	4.8%	200 mV	5.4%
		250	5.4%	6.0%	250 mV	6.5%

13.5.5 Charger status readback and error indication

The status of the QCC3095 VFBGA charger can be read by application software.

Table 13-13 Charger status and error indication

Charger status	Description
TRICKLE_CHARGE	Charger is in the Trickle Charge phase.
PRE_CHARGE	Charger is in the Pre-Charge phase.
FAST_CHARGE	Charger is in the Fast Charge phase.
STANDBY	Charger is in Standby.
HEADROOM_ERROR	Charger has error due to insufficient headroom (VCHG-VBAT).
VBAT_OVERVOLT_ERROR	Charger has error due to VBAT overvoltage.
NO_POWER	Charger has no VCHG supply present.
DISABLED_ERROR	Charger has not been enabled but VCHG is present.

Other error codes may be returned if the requested charger setup is not valid (for example if too high a charge current is requested for the configuration). For details on error codes, see application software documentation.

13.5.6 Charger headroom regions and errors

The QCC3095 VFBGA charger performance is affected by the headroom (defined as VCHG-VBAT) available to the charger. The headroom has three regions listed in Table 13-14.

Table 13-14 Headroom regions

Headroom region	Description	Charger
NORMAL_HEADROOM	VCHG-VBAT greater than 550mV	Operates as normal
REDUCED_HEADROOM	VCHG-VBAT below 550mV but greater than HEADROOM_ERROR threshold (falling) parameter	Operates but charge current may be reduced. Normal operation resumes if headroom rises again into the NORMAL_HEADROOM region
HEADROOM_ERROR	VCHG-VBAT below HEADROOM_ERROR threshold (falling) parameter	Stops operation and reports HEADROOM_ERROR

Table 13-15 Charger headroom parameters

Charger headroom error parameter	Min	Typ	Max	Unit
HEADROOM_ERROR threshold (falling)	30	65	100	mV
HEADROOM_ERROR threshold (rising)	95	140	190	mV

13.5.7 Charger overvoltage errors

The QCC3095 VFBGA charger has a protection circuit which latches off the charger and reports VBAT_OVERVOLT_ERROR if it detects the voltage on VBAT exceeds the VBAT_OVERVOLT_ERROR threshold (rising) value listed in Table 13-16.

The charger can be reset after an error by issuing a command to disable then re-enable the charger.

The VBAT_OVERVOLT_ERROR detection is sensitive and can be triggered when first restarting charge into a cell which is deeply discharged and whose battery protection circuit has opened, effectively disconnecting the battery from the charger. If this occurs, normal charger operation can be re-started by issuing a command to disable then re-enable the charger. Some battery protection circuits require additional steps to be taken to reset them and restore charging, such as ensuring no further cell discharge occurs during this charger reset.

Table 13-16 Charger overvoltage parameters

Charger VBAT overvoltage parameter	Min	Typ	Max	Unit
VBAT_OVERVOLT_ERROR threshold (rising)	4.65	4.70	4.75	V
VBAT_OVERVOLT_ERROR hysteresis	-	100	-	mV
VBAT_OVERVOLT_ERROR threshold (falling)	4.55	4.60	4.65	V

13.5.8 Charge phase timeout

The QCC3095 VFBGA charger application software can be configured with separate time limits for pre-charge and Fast charge phases. If these timers are enabled the charger will be disabled if for any reason the charger exceeds the set limit in that charge phase.

For details on how to set timeouts, see application software documentation.

13.5.9 Application VBAT voltage measurement

The QCC3095 VFBGA application software can measure the battery voltage on the VBAT pin and this information is typically used to provide a charge level indication to the user.

This facility is independent to the hardware voltage detection methods used as part of the charger system functionality.

For details on how to read the VBAT voltage, see application software documentation.

Table 13-17 Application VBAT voltage measurement accuracy

Measurement	Min	Typ	Max	Unit
Application VBAT voltage measurement accuracy	-	± 1	± 1.5	%

13.5.10 Battery protection

Deeply discharging a Li-ion battery for a long time can cause irreversible damage, leading to excessive heating on a subsequent charge cycle.

To prevent this deep discharge, customer application software can read the VBAT voltage periodically and should turn off the system typically around 3.0 V.

QTIL strongly recommends that all applications include a battery protection IC (normally built into the battery pack or immediately after the battery connects to the PCB) as a secondary level of protection, and this is often required by standards such as IEC62368. This protection device typically disconnects the battery cell if the voltage drops too low, or goes too high, and also protects against overcurrent in the connections between QCC3095 VFBGA and the cell.

If the cells battery protection switch has opened and charging is started, a VBAT_OVERVOLT_ERROR error may be seen.

Related Information

"Charger overvoltage errors" on page 83

14 QCC3095 VFBGA example application schematic

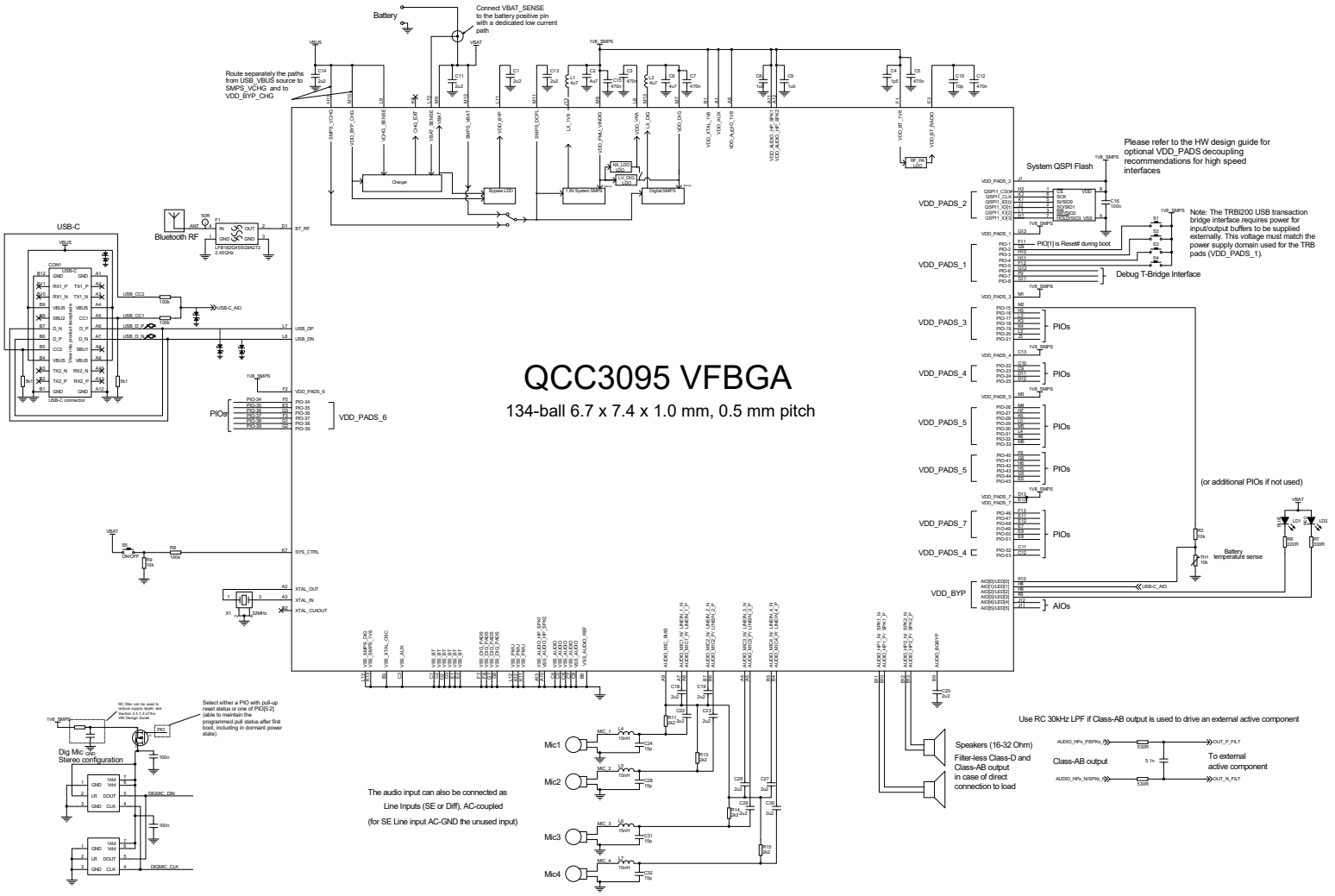


Figure 14-1 QCC3095 VFBGA example application schematic

15 Electrical characteristics

15.1 Absolute maximum ratings

Parameter	Pin	Min	Max	Unit
Storage temperature	-	-40	85	°C
Supply voltage				
VCHG[a]	CHG_EXT	-0.4	6.5	V
	LX_1V8			
	LX_DIG			
	SMPS_DCPL			
	SMPS_VCHG			
	VCHG_SENSE			
	VDD_BYP_CHG			
Battery	SMPS_VBAT	-0.4	4.8	V
	VBAT			
	VBAT_SENSE			
3.3 V	USB_DN	-0.4	3.8	V
	USB_DP			
	VDD_BYP			
	AUDIO_MIC_BIAS			
1.8 V	AUDIO_BGBYP	-0.4	2.1	V
	AUDIO_MIC1_N/ LINEIN_1_N			
	AUDIO_MIC1_P/ LINEIN_1_P			
	AUDIO_MIC2_N/ LINEIN_2_N			
	AUDIO_MIC2_P/ LINEIN_2_P			
	AUDIO_MIC3_N/ LINEIN_3_N			
	AUDIO_MIC3_P/ LINEIN_3_P			
	AUDIO_MIC4_N/ LINEIN_4_N			
	AUDIO_MIC4_P/ LINEIN_4_P			
	VDD_AUDIO_1V8			
	VDD_AUDIO_HP_SPK1			
	VDD_AUDIO_HP_SPK2			
	VDD_AUX			
	VDD_BT_1V8			
	VDD_PMU_VINDIG			
	VDD_XTAL_1V8			
	XTAL_CLKOUT			

[a] VCHG pins are tolerant of transients to 7.0 V of up to 10 ms. The steady state maximum is 6.5 V.

Parameter	Pin	Min	Max	Unit
1.8 V	AUDIO_HP1_N/ SPK1_N	-0.4	2.1	V
	AUDIO_HP1_P/ SPK1_P			
	AUDIO_HP2_N/ SPK2_N			
	AUDIO_HP2_P/ SPK2_P			
Digital I/O	PIO[53:15, 8:2]	-0.3	3.6	V
	QSPI1_CLK			
	QSPI1_CS0#			
	QSPI1_IO[3:0]			
	PIO[1]			
	VDD_PADS_7:1			
	AIO/LED[5:0] (Disabled / Digital Input / Open Drain Output Modes)	0	6.5	V
	AIO/LED[5:0] (AIO Mode)	0	1.95	V
	SYS_CTRL	-0.4	4.8	V
1.6 V	VDD_BT_RADIO	-0.4	2.1	V
0.95 V	XTAL_IN	-0.4	1.4	V
	XTAL_OUT			
0.7/0.8/0.9 V	VDD_DIG	-0.4	1.4	V
0.7 V	VDD_VKA			
All ground / VSS pads	-	-0.4	0.4	V

Parameter	Pin	Min	Max	Unit
DC Voltage	BT_RF	0	0	V
Radio Receive	BT_RF	-0.4	0.4	V
Radio Transmit (3:1 VSWR)	BT_RF	-1.6	1.6	V

CAUTION Stressing the device beyond the Absolute Maximum Ratings may cause instantaneous and permanent damage.

Device performance is not guaranteed beyond the Recommended Operating Conditions.

Prolonged exposure beyond the Recommended Operating Conditions may permanently affect device reliability and/or performance.

15.2 Recommended operating conditions

Parameter	Pin	Min	Typ	Max	Unit
Operating temperature range	-	-40	25	85	°C
Charger operating temperature range	-	-10	25	85	°C
Supply voltage					
5 V (USB VBUS)	CHG_EXT	4.75 / 4.00[a]	5.00	6.50	V
	SMPS_VCHG				
	VCHG_SENSE				
	VDD_BYP_CHG				
	SMPS_DCPL	2.8	3.7 / 5.0	6.5	V
	LX_1V8	0	3.7 / 5.0	6.5	V
	LX_DIG				
Battery	SMPS_VBAT	3.0 / 2.8[b]	3.7	4.6	V
	VBAT				
	VBAT_SENSE				
3.3 V	VDD_BYP	2.8	2.9 / 3.3	3.5	V
	AUDIO_MIC_BIAS	0	-	2.3	
	USB_DN	0	-	3.6	
	USB_DP				
1.8 V	VDD_AUDIO_1V8	1.65	1.80	1.95	V
	VDD_AUDIO_HP_SPK1				
	VDD_AUDIO_HP_SPK2				
	VDD_AUX				
	VDD_BT_1V8				
	VDD_PMU_VINDIG				
	VDD_XTAL_1V8				
	XTAL_CLKOUT				
	AUDIO_BGBYP	0	-	1.95	V
	AUDIO_MIC1_N/ LINEIN_1_N				
	AUDIO_MIC1_P/ LINEIN_1_P				
	AUDIO_MIC2_N/ LINEIN_2_N				
	AUDIO_MIC2_P/ LINEIN_2_P				
	AUDIO_MIC3_N/ LINEIN_3_N				
	AUDIO_MIC3_P/ LINEIN_3_P				
	AUDIO_MIC4_N/ LINEIN_4_N				
	AUDIO_MIC4_P/ LINEIN_4_P				

[a] Minimum input voltage of 4.75 V is required for full specification. Li-ion charger operates at reduced specification from 4.00 V.
[b] Recommended software power-off threshold at 3.0 V. Device operates down to 2.8 V.

Parameter	Pin	Min	Typ	Max	Unit
1.8 V	AUDIO_HP1_N/ SPK1_N	0	-	1.95	V
	AUDIO_HP1_P/ SPK1_P				
	AUDIO_HP2_N/ SPK2_N				
	AUDIO_HP2_P/ SPK2_P				
Digital I/O	VDD_PADS_7:1	1.7	1.8	3.6	V
	PIO[53:15, 8:2]	0	-	VDD_PADS	V
	QSPI1_CLK				
	QSPI1_CS0#				
	QSPI1_IO[3:0]				
	PIO[1]	0	-	VDD_BYP	V
	AIO/LED[5:0] (Disabled / Digital Input / Open Drain Output Modes)	0	-	6.5	V
	AIO/LED[5:0] (AIO Mode)	0	-	1.95	V
	SYS_CTRL	0	-	4.6	V
1.6 V	VDD_BT_RADIO	1.5	-	1.7	V
0.95 V	XTAL_IN	0.81	0.95	0.99	V
	XTAL_OUT				
0.7/0.8/0.9 V	VDD_DIG	0.63/0.72/0.81	0.7/0.8/0.9	0.85/0.95/1.05	V
0.7 V	VDD_VKA	0.63	0.7	0.85	V
All ground / VSS pads	-	0	-	0	V

15.3 Battery input pin specification

Battery specifications common to all regulators.

VBAT	Min	Typ	Max	Unit
Operating voltage	2.8	3.7	4.6	V
Boot voltage	3.0	-	4.6	V
Software power-off threshold (configurable in application)	-	3.0	-	V
USB dead/weak battery rising threshold	3.14	3.30	3.46	V
USB dead/weak battery hysteresis	50	-	120	mV

15.4 Charger input pin specification

VCHG specifications common to all regulators.

VCHG	Min	Typ	Max	Unit
Operating voltage (full charger specification)	4.75	5.00	5.50[a]	V
Operating voltage (reduced charger specification)[b]	4.00	5.00	5.50[a]	V
VCHG_PRESENT rising threshold	3.4	3.6	4.0	V
VCHG_PRESENT hysteresis	30	-	115	mV
VCHG_PLUGGED rising threshold	2.4	2.9	3.3	V
VCHG_PLUGGED hysteresis	100	-	600	mV
Full operating range[a]	VCHG_ PRESENT	-	6.50	V
On chip pull-down (disabled when VCHG_PRESENT = 1, configurable by MIB key)	10	20	30	kΩ
Hold time to transition from Off to Active state	-	20	32	ms

[a] The VCHG pin is tolerant of voltages up to 6.5 V, but the standard specified operating range of the charger is up to 5.5 V. With VCHG at 6.5 V, the typical battery charge current will be approximately 5% greater than at 5.5 V.
[b] For details on how VCHG to VBAT headroom affects charger operation, see *Related Information*.

RELATED INFORMATION

"Charger headroom regions and errors" on page 83

15.5 Battery charger

For details, see *Related Information*.

NOTE Unless specified otherwise, all specifications are applicable over the charger operating temperature range stated in *Recommended operating conditions*.

RELATED INFORMATION

"General charger operation" on page 76

15.6 Regulator enable

SYS_CTRL	Min	Typ	Max	Unit
Rising switching threshold	1.6[a]	-	-	V
Falling switching threshold	0	-	0.4[b]	V
Hold time to transition from Off to Active state	-	20	32	ms

[a] Voltage rising to 1.6 V or above is guaranteed to be detected as a rising edge.
[b] Voltage dropping to 0.4 V or below is guaranteed to be detected as a falling edge.

15.7 Bypass LDO

Bypass LDO	Min	Typ	Max	Unit
Input voltage	VDD_BYP_BAT / VDD_BYP_CHG			V
HP mode				
Output voltage, 3.3 V mode, > 0.3 V headroom	3.2	3.3	3.5	V
Output voltage, 2.9 V mode, > 0.3 V headroom	2.8	2.9	3.05[a]	V
Pass device resistance when headroom < 0.3 V	-	-	6	Ω
Output current	-	-	50	mA
Current available for external use	-	-	25	mA
ULP mode[b]				
Output voltage, 2.9 V mode[c]	2.7	2.9	3.1[a]	V
Output voltage, 2.65 V mode[d]	2.49	2.65	2.85[a]	V
Maximum load current	-	-	1	mA

[a] 3.5 V during transition between system power states.
[b] ULP mode is automatically entered in Deep Sleep and Dormant states, application software can disable automatic mode switching.
[c] Typically used for Deep Sleep state.
[d] Typically used for Dormant state.

NOTE By default the bypass LDO will switch automatically between 2.9 V and 3.3 V modes depending on the use case. If a constant operation in 3.3 V mode is required, the MIB key BypassLdoForce3v3 can be set to True.

15.8 1.8 V SMPS

1.8 V SMPS					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Input supply	-	SMPS_VCHG / SMPS_VBAT			-
DC output voltage	-	1.71	1.8	1.89	V
Output voltage	Including transients	1.65	1.8	1.95	V
Transient load step response (PWM)	-	-0.4	-	0.4	mV/mA
Output filter inductance	-	3.76[a]	4.7	5.6	µH
Inductor saturation current	-	-	600	-	mA
Inductor DC resistance	-	-	290	-	mΩ
Output filter capacitance	-	3.76[a]	4.7	9	µF
Total capacitance on the SMPS output	-	7.74	-	16	µF
PWM mode					
Output current	-	-	-	350	mA
Current available for external use	-	-	-	100	mA
Overcurrent protection threshold	-	350	-	1500	mA
Peak conversion efficiency	-	-	88	-	%
Switching frequency	-	1.9	2.0	2.1	MHz
PFM mode					
Output current	-	-	-	40	mA
Peak conversion efficiency	-	-	85	-	%
ULP mode[b]					
Output current	-	-	-	40	mA
Current available for external use	-	-	-	30	mA
Peak conversion efficiency	-	-	85	-	%

[a] Including tolerances and derating
[b] ULP mode is used in Deep Sleep and Dormant modes. In Active mode, SMPS automatically switches between PFM and PWM based on the load.

15.9 Digital SMPS

Digital SMPS				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Input supply	SMPS_VCHG / SMPS_VBAT			-
DC output voltage (Active)	-	0.8/0.9	-	V
DC output voltage (Deep Sleep)	-	0.7/0.8	-	V
Output filter inductance	2.82[a]	4.7	5.6	µH
Inductor saturation current	-	500	-	mA
Inductor DC resistance	-	290	-	mΩ
Output filter capacitance	1.7[a]	4.7	5.64	µF

Digital SMPS				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Normal operation (PWM)				
Output current	-	-	250	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	1.9	2.0	2.1	MHz
PFM mode				
Peak conversion efficiency	-	85	-	%
ULP mode				
Peak conversion efficiency	-	85	-	%

[a] Including tolerances and derating

15.10 10-bit auxiliary ADC

10-bit auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
VDD_AUX_ADC[a]		1.746	1.800	1.854	V
Functional input voltage range[b]		0	-	VDD_AUX_ADC	V
Accuracy (Guaranteed monotonic)[c]	INL	-3	-	3	LSB
	DNL	-1	-	2	LSB
Offset		-1	-	1	LSB
Gain error		-1	-	1	%
Hardware conversion time[d]		-	10	-	µs
LED pad leakage		-1	-	1	µA
External pad capacitance for < 0.5 LSB error		0	40	-	pF

[a] Internal voltage reference.
[b] LSB size = VDD_AUX_ADC/1023.
[c] Accuracy guaranteed for input signal range: [4LSBs; Full scale - 4LSBs].
[d] Software may introduce additional delay.

15.11 Digital terminals

Digital terminals	Min	Typ	Max	Unit
VDD_PADS supply	1.7	1.8	3.6	V
VIL input logic level low	-	-	0.25 x VDD_PADS	V
VIH input logic level high	0.625 x VDD_PADS	-	-	V
Drive current (configurable)	2, 4, 8, 12	4	-	mA
VOL output logic level low, at configured drive current	-	-	0.22 x VDD_PADS	V
VOH output logic level high, at configured drive current	0.75 x VDD_PADS	-	-	V

Digital terminals	Min	Typ	Max	Unit
Strong pull (up and down)	50	70	125	kΩ
Weak pull (up and down)	729	1050	1350	kΩ

15.12 LED driver pads

LED driver pads		Min	Typ	Max	Unit
Open drain current	High impedance state	-	-	5	µA
	Current sink state	-	-	50	mA
LED pad resistance	V < 0.5 V	-	-	12	Ω
VIL input logic level low		-	-	0.4	V
VIH input logic level high		0.8	-	-	V

15.13 Application VBAT voltage measurement accuracy

Measurement	Min	Typ	Max	Unit
Application VBAT voltage measurement accuracy	-	± 1	± 1.5	%

15.14 PMU temperature sensor measurement accuracy

Measurement	Min	Typ	Max	Unit
PMU temperature sensor measurement accuracy	-	-	± 5	°C

16 Audio performance

QCC3095 VFBGA audio performance, includes data for:

- Digital-to-analog convertors
- Analog-to-digital convertors
- Microphone bias

16.1 Digital-to-analog converters

Table 16-1 lists Class-D DAC audio output data and Table 16-2 lists Class-AB DAC audio output data.

Table 16-1 Class-D DAC audio output

Parameter	Conditions	Min	Typ	Max	Unit
Input Sample Width	-	-	-	24	Bits
Input Sample Rate, F_{sample}	-	8	-	192	kHz
Output Power	0 dBFS, 32 Ω load -3 dBFS, 16 Ω load	-	-	30	mW
Load	-	16	32	30k	Ω
SNR	▪ F_{in} = 1 kHz ▪ F_{sample} = 48 kHz ▪ Input amplitude = 0 dBFS ▪ Analog gain = 0 dB ▪ B/W = 20 Hz to 20 kHz ▪ A-Weighted ▪ 32 Ω load	-	105.1	-	dB
THD+N	▪ F_{in} = 1 kHz ▪ F_{sample} = 48 kHz ▪ Input amplitude = 0 dBFS ▪ Analog gain = 0 dB ▪ B/W = 20 Hz to 20 kHz ▪ 32 Ω load	-	-90.1	-	dB
RMS noise	▪ F_{sample} = 48 kHz ▪ Input amplitude = - 200 dBFS ▪ Analog gain = 0 dB ▪ B/W = 20 Hz to 20 kHz ▪ A-Weighted ▪ 32 Ω load	-	5.48	-	µVrms

Parameter	Conditions	Min	Typ	Max	Unit
Stereo separation (crosstalk)	-	80	-	-	dB
Max capacitive load	Per terminal to ground	-	-	100	pF

Table 16-2 Class-AB DAC audio output

Parameter	Conditions		Min	Typ	Max	Unit
Input Sample Width	-		-	-	24	Bits
Input Sample Rate, F_{sample}	-		8	-	192	kHz
Output Power	0 dBFS, 32 Ω load -3 dBFS, 16 Ω load		-	-	30	mW
Load	-		16	32	30k	Ω
SNR	■ F_{in} = 1 kHz ■ F_{sample} = 48 kHz ■ Input amplitude = 0 dBFS ■ B/W = 20 Hz to 20 kHz ■ A-Weighted ■ 32 Ω load	**Analog gain (dB)**	**Min**	**Typ**	**Max**	**Unit**
		0	-	104.8	-	dB
		-6		103.9		
		-12		100.4		
	■ Software DRE mode	-		109.5		
	■ Quiet mode	0		120.0		
THD+N	■ F_{in} = 1 kHz ■ F_{sample} = 48 kHz ■ Input amplitude = 0 dBFS ■ B/W = 20 Hz to 20 kHz ■ 32 Ω load	0	-	-91.1	-	dB
		-6		-91.7		
		-12		-91.3		
RMS noise	■ F_{sample} = 48 kHz ■ Input amplitude = -200 dBFS ■ B/W = 20 Hz to 20 kHz ■ A-Weighted ■ 32 Ω load	0	-	5.69	-	µVrms
		-6		3.18		
		-12		2.39		
	■ Software DRE mode	-		3.23		
	■ Quiet mode	-		<1		
Stereo separation (crosstalk)	-		80	-	-	dB

NOTE For details on how to implement DAC Quiet Mode (DQM), see ADK Software Data Sheet.

16.2 Analog-to-digital converters

Table 16-3 lists high-quality (HQADC) single-ended audio input data and Table 16-4 lists high-quality (HQADC) differential audio input data.

Table 16-3 High-quality (HQADC) single-ended audio input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0 dB to 24 dB analog gain	-	20	-	kΩ
	27 dB to 39 dB analog gain	-	10	-	kΩ
SNR	▪ F_{in} = 1 kHz ▪ F_{sample} = 48 kHz ▪ Input amplitude = 2.4 V_{pk-pk} ▪ B/W = 20 Hz to 20 kHz ▪ A-Weighted	-	99.1	-	dB
THD+N	▪ F_{in} = 1 kHz ▪ F_{sample} = 48 kHz ▪ Input amplitude = 2.4 V_{pk-pk} ▪ B/W = 20 Hz to 20 kHz	-	-91.4	-	dB
Analog gain	3 dB steps	0	-	39	dB
Stereo separation (crosstalk)	-	80	-	-	dB

Table 16-4 High-quality (HQADC) differential audio input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0 dB to 24 dB analog gain	-	20	-	kΩ
	27 dB to 39 dB analog gain	-	10	-	kΩ
SNR	▪ F_{in} = 1 kHz ▪ F_{sample} = 48 kHz ▪ Input amplitude = 2.4 V_{pk-pk} ▪ B/W = 20 Hz to 20 kHz ▪ A-Weighted	-	99.2	-	dB
THD+N	▪ F_{in} = 1 kHz ▪ F_{sample} = 48 kHz ▪ Input amplitude = 2.4 V_{pk-pk} ▪ B/W = 20 Hz to 20 kHz	-	-95.0	-	dB
Analog gain	3 dB steps	0	-	39	dB
Stereo separation (crosstalk)	-	80	-	-	dB

16.3 Microphone bias

Table 16-5 Microphone bias

Parameter	Conditions	Min	Typ	Max	Unit
Output voltage (Tunable, step = 0.1 V)	-	1.5	-	2.1	V
Output current capability	-	0.07	-	6.00	mA
DC accuracy	-	-60	-	60	mV
Output noise	B/W = 20 Hz → 20 kHz Unweighted	4.5	5.1	7.3	μVrms
Crosstalk between microphones	Using recommended application circuit	-	80	-	dB
Load capacitance [a]	From parasitic PCB routing and package	-	-	0.1	nF

[a] If a greater amount of decoupling capacitance is required at the microphone(s), a total capacitance up to 2.2 μF (max) can be used provided a 10 Ω (min) resistor is inserted between the mic bias pin and the capacitor (see *QCC3095 VFBGA Hardware Design Guide* (80-74170-1)).

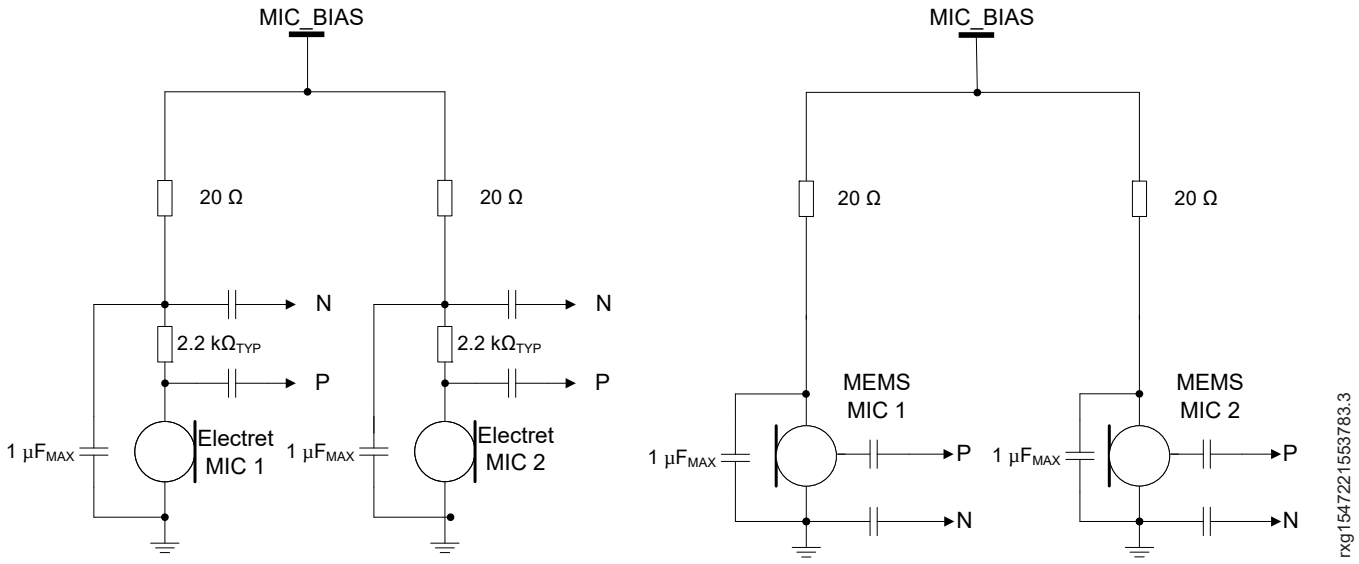


Figure 16-1 Microphone bias configuration for electret microphones (left) and MEMS microphones (right)

If using MEMS microphones, power these from either:

- the 1.8 V SMPS rail via a FET switch (to limit deep sleep current consumption)
- a PIO (if the power consumption of the microphones is sufficiently low)
- the microphone bias regulator

NOTE If the microphone bias supply is used and additional decoupling is required at the MEMS microphones a total capacitance up to 2.2 µF (max) can be used provided a 10 Ω (min) resistor is inserted between AUDIO_MIC_BIAS and the capacitor.

17 Bluetooth performance

17.1 Bluetooth radio characteristics: Basic Rate

Table 17-1 Basic rate transmitter performance at 25°C

Radio characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Maximum RF transmit power		[a]	13.5	15.0	-	≤20	dBm
ACP	F = F_0 ± 2 MHz	[bc]	-	-38	-20	≤-20	dBm
	F = F_0 ± 3 MHz	[bc]	-	-45	-40	≤-40	dBm
	F > F_0 ± 3 MHz	[bc]	-	-57	-40	≤-40	dBm
2nd harmonic content		[d]	-	-29	-	≤-15	dBm
3rd harmonic content		[d]	-	-33	-	≤-17	dBm

[a] QCC3095 VFBGA firmware is set to target 15 dBm. Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
[b] Measured at F_0 = 2441 MHz.
[c] Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq$ -20 dBm.
[d] Conducted measurement at RF port. Use of an appropriate filter will attenuate transmit harmonics.

Table 17-2 Basic rate receiver performance at 25°C

Radio characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Sensitivity at 0.1% BER	2.402	[a]	-	-97.0	-95.0	≤-70	dBm
	2.441	[a]	-	-97.0	-95.0		
	2.480	[a]	-	-97.0	-95.0		
Maximum received signal at 0.1% BER		-	-20	≥-9	-	≥-20	dBm

[a] Dirty transmitter used.

17.2 Bluetooth radio characteristics: Enhanced Data Rate

Table 17-3 Enhanced data rate transmitter performance at 25°C

Radio characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Maximum RF Transmit Power	π/4 DQPSK	-	10.0	11.5	-	≤20	dBm
	8DPSK	-	10.0	11.5	-	≤20	dBm
π/4 DQPSK modulation accuracy	RMS DEVM	a	-	5.0	20	≤20	%
	99% DEVM	a	-	9.0	30	≤30	%
	Peak DEVM	a	-	12.0	35	≤35	%
8DPSK modulation accuracy	RMS DEVM	a	-	5.0	13	≤13	%
	99% DEVM	a	-	9.5	20	≤20	%
	Peak DEVM	a	-	12.5	25	≤25	%
In-band spurious emissions	$F < F_0$ - 3 MHz	bc	-	-49	-40	≤-40	dBm
	$F = F_0$ - 3 MHz	bc	-	-40	-40	≤-40	dBm
	$F = F_0$ - 2 MHz	bc	-	-27	-20	≤-20	dBm
	$F = F_0$ - 1 MHz	bc	-	-37	-26	≤-26	dB
	$F = F_0$ + 1 MHz	bc	-	-38	-26	≤-26	dB
	$F = F_0$ + 2 MHz	bc	-	-30	-20	≤-20	dBm
	$F = F_0$ + 3 MHz	bc	-	-39	-40	≤-40	dBm
	$F > F_0$ + 3 MHz	bc	-	-49	-40	≤-40	dBm

[a] Modulation accuracy utilizes differential error vector magnitude with tracking of the carrier frequency.
[b] Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq$ -20 dBm.
[c] Bluetooth specification values are for 8DPSK.

Table 17-4 Enhanced data rate receiver performance at 25°C

Radio characteristics, VBAT = 3.7 V		Notes	Modulation	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Sensitivity at 0.01% BER	Ch 0	a	π/4 DQPSK	-	-96.5	-94.5	≤-70	dBm
	Ch 39	a	π/4 DQPSK	-	-96.5	-94.5		
	Ch 78	a	π/4 DQPSK	-	-96.5	-94.5		
	Ch 0	a	8DPSK	-	-90.0	-88.0	≤-70	dBm
	Ch 39	a	8DPSK	-	-90.0	-88.0		
	Ch 78	a	8DPSK	-	-90.0	-88.0		
Maximum received signal at 0.1% BER		-	π/4 DQPSK	-20	≥-9	-	≥-20	dBm
		-	8DPSK	-20	≥-9	-	≥-20	dBm

[a] Dirty transmitter used.

17.3 Bluetooth radio characteristics: Low Energy 1 Mb/s

Table 17-5 Bluetooth Low Energy 1 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Maximum RF transmit power		[a]	13.0	14.5	-	-20 ≤ P_{AVG} ≤ +20	dBm
In-band spurious emissions	F = F_0 ± 2 MHz	[bc]	-	-36	-20	≤-20	dBm
	F = F_0 ± 3 MHz	[bc]	-	-46	-30	≤-30	dBm
	F > F_0 ± 3 MHz	[bc]	-	-58	-30	≤-30	dBm
2nd harmonic content		[d]	-	-29	-	-	dBm
3rd harmonic content		[d]	-	-33	-	-	dBm

[a] Output power is measured at the chip pin. QCC3095 VFBGA firmware maintains the transmit power within Bluetooth v5.4 RF-PHY Test Specification limits. Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
[b] Measured at F_0 = 2440 MHz.
[c] Exceptions in up to three bands are allowed. For exceptions, P_{TX} ≤ -20 dBm.
[d] Conducted measurement at RF port. Use of an appropriate filter will attenuate transmit harmonics.

Table 17-6 Bluetooth Low Energy 1 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Sensitivity at 30.8% PER	2.402	[a]	-	-100.0	-98.0	≤-70	dBm
	2.440	[a]	-	-100.0	-98.0		
	2.480	[a]	-	-100.0	-98.0		
Maximum received signal at 30.8% PER		-	-20	≥-9	-	≥-20	dBm

[a] Measured using test packets with 37 octet payload.

17.4 Bluetooth radio characteristics: Low Energy 2 Mb/s

Table 17-7 Bluetooth Low Energy 2 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Maximum RF transmit power		[a]	13.0	14.5	-	$-20 \leq P_{AVG} \leq +20$	dBm
In-band spurious emissions	$F = F_0 \pm 4$ MHz	[bc]	-	-44	-20	≤-20	dBm
	$F = F_0 \pm 5$ MHz	[bc]	-	-49	-20	≤-20	dBm
	$F = F_0 \pm 6$ MHz	[bc]	-	-53	-30	≤-30	dBm
	$F > F_0 \pm 6$ MHz	[bc]	-	-60	-30	≤-30	dBm
2nd harmonic content		[d]	-	-29	-	-	dBm
3rd harmonic content		[d]	-	-33	-	-	dBm

[a] Output power is measured at the chip pin. QCC3095 VFBGA firmware maintains the transmit power within Bluetooth v5.4 RF-PHY Test Specification limits. Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
[b] Measured at F_0 = 2440 MHz.
[c] Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq -20$ dBm.
[d] Conducted measurement at RF port. Use of an appropriate filter will attenuate transmit harmonics.

Table 17-8 Bluetooth Low Energy 2 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Sensitivity at 30.8% PER	2.402	[a]	-	-97.0	-95.0	≤-70	dBm
	2.440	[a]	-	-97.0	-95.0		
	2.480	[a]	-	-97.0	-95.0		
Maximum received signal at 30.8% PER		-	-10	≥-9	-	≥-10	dBm

[a] Measured using test packets with 37 octet payload.

17.5 Qualcomm Bluetooth High Speed Link radio characteristics: 2 Mb/s

Table 17-9 Qualcomm Bluetooth High Speed Link 2 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Specification	Unit
Maximum RF transmit power		a	11.5	13.0	-	≤20	dBm
In-band spurious emissions	F = F_0 ± 4 MHz	bc	-	-36	-20	≤-20	dBm
	F = F_0 ± 5 MHz	bc	-	-35	-20	≤-20	dBm
	F = F_0 ± 6 MHz	bc	-	-42	-30	≤-30	dBm
	F > F_0 ± 6 MHz	bc	-	-53	-30	≤-30	dBm
Modulation accuracy	RMS DEVM	d	-	2.5	12	≤12	%
	99% DEVM	d	-	5.0	23	≤23	%
	Peak DEVM	d	-	7.0	35	≤35	%

a Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
b Measured at F_0 = 2440 MHz.
c Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq$ -20 dBm.
d Modulation accuracy utilizes differential error vector magnitude with tracking of the carrier frequency.

Table 17-10 Qualcomm Bluetooth High Speed Link 2 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Specification	Unit
Sensitivity at 30.8% PER	2.402	ab	-	-101.5	-99.5	≤-93	dBm
	2.440	ab	-	-101.5	-99.5		
	2.480	ab	-	-101.5	-99.5		

a Dirty transmitter used.
b Measured using test packets with 35 byte payload.

17.6 Qualcomm Bluetooth High Speed Link radio characteristics: 3 Mb/s

Table 17-11 Qualcomm Bluetooth High Speed Link 3 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Specification	Unit
Maximum RF transmit power		a	11.5	13.0	-	≤20	dBm
In-band spurious emissions	F = F_0 ± 4 MHz	bc	-	-35	-20	≤-20	dBm
	F = F_0 ± 5 MHz	bc	-	-35	-20	≤-20	dBm
	F = F_0 ± 6 MHz	bc	-	-42	-30	≤-30	dBm
	F > F_0 ± 6 MHz	bc	-	-53	-30	≤-30	dBm
Modulation accuracy	RMS DEVM	d	-	2.5	10	≤10	%
	99% DEVM	d	-	5.0	20	≤20	%
	Peak DEVM	d	-	7.0	30	≤30	%

a Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
b Measured at F_0 = 2440 MHz.
c Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq$ -20 dBm.
d Modulation accuracy utilizes differential error vector magnitude with tracking of the carrier frequency.

Table 17-12 Qualcomm Bluetooth High Speed Link 3 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Specification	Unit
Sensitivity at 30.8% PER	2.402	ab	-	-99.0	-97.0	≤-90	dBm
	2.440	ab	-	-99.0	-97.0		
	2.480	ab	-	-99.0	-97.0		

a Dirty transmitter used.
b Measured using test packets with 35 byte payload.

17.7 Qualcomm Bluetooth High Speed Link radio characteristics: 4 Mb/s

Table 17-13 Qualcomm Bluetooth High Speed Link 4 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Specification	Unit
Maximum RF transmit power		a	11.5	13.0	-	≤20	dBm
In-band spurious emissions	F = F_0 ± 4 MHz	bc	-	-35	-20	≤-20	dBm
	F = F_0 ± 5 MHz	bc	-	-36	-20	≤-20	dBm
	F = F_0 ± 6 MHz	bc	-	-42	-30	≤-30	dBm
	F > F_0 ± 6 MHz	bc	-	-53	-30	≤-30	dBm
Modulation accuracy	RMS DEVM	d	-	2.5	8	≤8	%
	99% DEVM	d	-	4.5	17.5	≤17.5	%
	Peak DEVM	d	-	6.5	22	≤22	%

a Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
b Measured at F_0 = 2440 MHz.
c Exceptions in up to three bands are allowed. For exceptions, P_{TX} ≤ -20 dBm.
d Modulation accuracy utilizes differential error vector magnitude with tracking of the carrier frequency.

Table 17-14 Qualcomm Bluetooth High Speed Link 4 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Specification	Unit
Sensitivity at 30.8% PER	2.402	ab	-	-94.5	-92.5	≤-86	dBm
	2.440	ab	-	-94.5	-92.5		
	2.480	ab	-	-94.5	-92.5		

a Dirty transmitter used.
b Measured using test packets with 35 byte payload.

17.8 Qualcomm Bluetooth High Speed Link radio characteristics: 5 Mb/s

Table 17-15 Qualcomm Bluetooth High Speed Link 5 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Specification	Unit
Maximum RF transmit power		a	11.5	13.0	-	≤20	dBm
In-band spurious emissions	F = F_0 ± 4 MHz	bc	-	-34	-20	≤-20	dBm
	F = F_0 ± 5 MHz	bc	-	-35	-20	≤-20	dBm
	F = F_0 ± 6 MHz	bc	-	-41	-30	≤-30	dBm
	F > F_0 ± 6 MHz	bc	-	-52	-30	≤-30	dBm
Modulation accuracy	RMS DEVM	d	-	3.0	8	≤8	%
	99% DEVM	d	-	5.5	17.5	≤17.5	%
	Peak DEVM	d	-	8.0	20	≤20	%

a Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
b Measured at F_0 = 2440 MHz.
c Exceptions in up to three bands are allowed. For exceptions, P_{TX} ≤ -20 dBm.
d Modulation accuracy utilizes differential error vector magnitude with tracking of the carrier frequency.

Table 17-16 Qualcomm Bluetooth High Speed Link 5 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Specification	Unit
Sensitivity at 30.8% PER	2.402	ab	-	-92.0	-90.0	≤-84	dBm
	2.440	ab	-	-92.0	-90.0		
	2.480	ab	-	-92.0	-90.0		

a Dirty transmitter used.
b Measured using test packets with 35 byte payload.

17.9 Qualcomm Bluetooth High Speed Link radio characteristics: 6 Mb/s

Table 17-17 Qualcomm Bluetooth High Speed Link 6 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.7 V		Notes	Min	Typ	Max	Specification	Unit
Maximum RF transmit power		a	11.5	13.0	-	≤20	dBm
In-band spurious emissions	F = F_0 ± 4 MHz	bc	-	-34	-20	≤-20	dBm
	F = F_0 ± 5 MHz	bc	-	-35	-20	≤-20	dBm
	F = F_0 ± 6 MHz	bc	-	-41	-30	≤-30	dBm
	F > F_0 ± 6 MHz	bc	-	-52	-30	≤-30	dBm
Modulation accuracy	RMS DEVM	d	-	3.0	8	≤8	%
	99% DEVM	d	-	6.0	17.5	≤17.5	%
	Peak DEVM	d	-	8.0	20	≤20	%

a Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
b Measured at F_0 = 2440 MHz.
c Exceptions in up to three bands are allowed. For exceptions, P_{TX} ≤ -20 dBm.
d Modulation accuracy utilizes differential error vector magnitude with tracking of the carrier frequency.

Table 17-18 Qualcomm Bluetooth High Speed Link 6 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.7 V	Frequency (GHz)	Notes	Min	Typ	Max	Specification	Unit
Sensitivity at 30.8% PER	2.402	ab	-	-89.0	-87.0	≤-81	dBm
	2.440	ab	-	-89.0	-87.0		
	2.480	ab	-	-89.0	-87.0		

a Dirty transmitter used.
b Measured using test packets with 35 byte payload.

18 Power consumption

For QCC3095 VFBGA power consumption data, see the relevant ADK release documentation.

19 RoHS compliance

This device meets the substance restriction requirement of the EU RoHS directive.

For further information, refer to the *Product Material Declaration* (PMD) for this device on www.qualcomm.com.

20 Software development and tools

QTIL provides a Qualcomm® MultiCore Development Environment (QMDE), device firmware, and an example application within an ADK. These support software development on QCC3095 VFBGA, enabling development of a range of products including:

- Standalone audio units such as wireless speakers.

NOTE Reference applications are supplied by QTIL, these support a subset of the functionality included in the firmware.

20.1 Qualcomm® Multicore Development Environment

The QMDE provides features for building software and debugging it on the hardware. QMDE includes an editor and tools to build, deploy, and debug applications. QMDE works with multiple ADKs as a single unified debugger.

20.2 Application Development ToolKit

The ADK Toolkit provides all the tools necessary to build, debug, and deploy applications. Reference applications can be downloaded from ChipCode™.

For additional tools and the complete ADK documentation set, go to www.qualcomm.com.

21 Carrier, storage, and handling information

Carrier, storage, and handling information describes how to safely transport QCC3095 VFBGA devices.

21.1 Carrier

The QCC3095 VFBGA carrier system is tape and reel.

21.1.1 Tape and reel information

All QTIL tape carrier systems conform to EIA-481 standards.

Figure 21-1 and Table 21-1 show and list part orientation, maximum number of devices per reel, and dimensions for the QCC3095 VFBGA tape carrier.

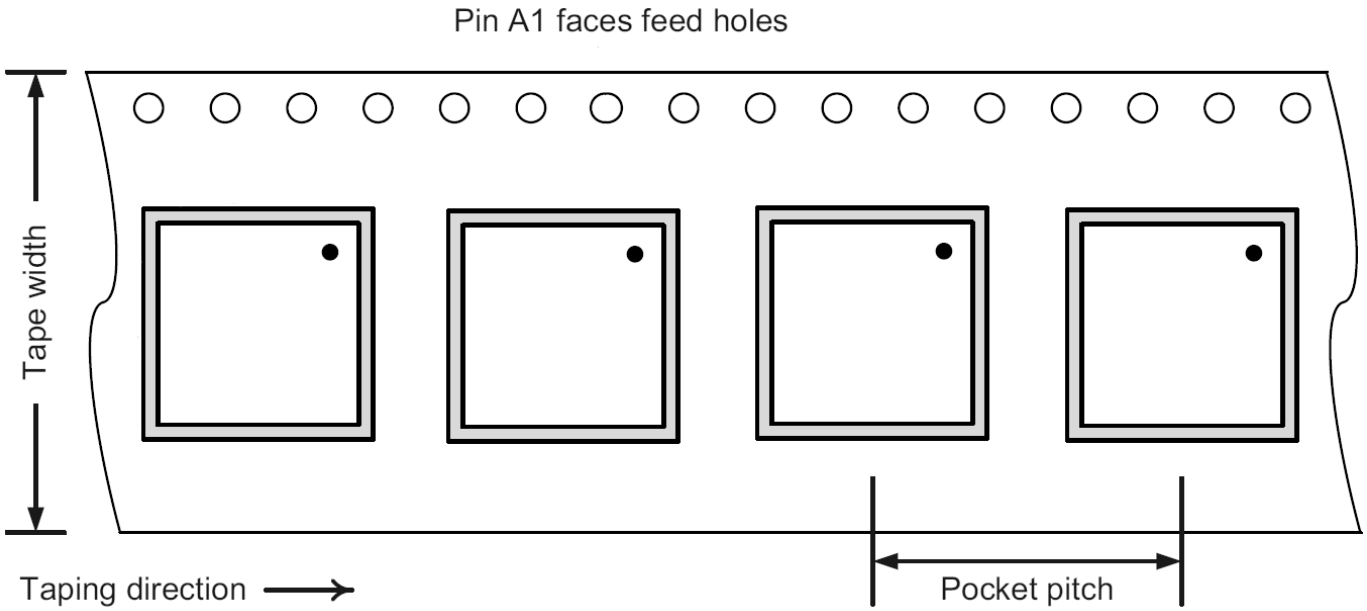


Figure 21-1 QCC3095 VFBGA carrier tape and part orientation

Table 21-1 QCC3095 VFBGA carrier tape dimensions

Tape feed:	Single	**Reel diameter:**	330 mm	**Tape width:**	16 mm
Units per reel:	2000	**Hub diameter:**	178 mm	**Pocket pitch:**	12 mm

Figure 21-2 shows recommendations for tape handling.

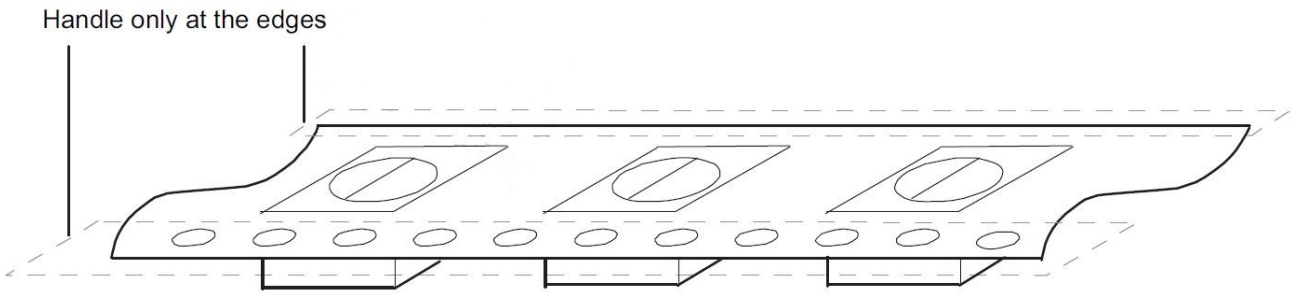


Figure 21-2 Tape handling recommendations

21.2 Storage

QCC3095 VFBGA device storage includes:

- Bagged storage conditions
- Out-of-bag duration

21.2.1 Bagged storage conditions

QCC3095 VFBGA devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. For expected shelf life, see *IC Products Packing Method* (80-VK055-1).

21.2.2 Out-of-bag duration

Out-of-bag duration is the time a device can be on the factory floor before installation onto a PCB. It is defined by the device moisture sensitivity level (MSL) rating, see *Related Information*.

RELATED INFORMATION

"Moisture sensitivity level" on page 33

21.3 Handling

QCC3095 VFBGA device handling includes:

- Baking
- Electrostatic discharge

21.3.1 Baking

QCC3095 VFBGA devices require baking if storage conditions are exceeded. QCC3095 VFBGA devices do not require baking if storage conditions are not exceeded. Baking conditions are specified on the moisture-sensitive caution label attached to each bag. For details, see *IC Products Packing Method* (80-VK055-1).

CAUTION If baking is required, QCC3095 VFBGA devices must be transferred into trays that can be baked to at least 125°C. QCC3095 VFBGA devices should not be baked in tape and reel carriers at any temperature.

21.3.2 Electrostatic discharge

ESD occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTIL recommends implementing ESD control program such as ANSI/ESD S20.20-2014 or IEC 61340-5 (required for electronics manufacturing environment) to safely handle ESD sensitive products.

For QCC3095 VFBGA ESD ratings, see *Related Information*.

Related Information

"Silicon reliability results" on page 115

21.4 Bar code label and packing for shipment

For all packing-related information, including bar code label details, see *IC Products Packing Method* (80-VK055-1).

22 Part reliability

QCC3095 VFBGA part reliability, includes:

- Silicon reliability results
- Package reliability results
- Board level reliability results

NOTE Foundry source TSMC F15.

22.1 Silicon reliability results

Table 22-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	1359	Pass DPPM < 1000 DPPM
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	717	Pass 16.4 FIT[a]
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	717	61
ESD – Human-body model (HBM) rating JS-001-2017 (Total samples from one wafer lot)	3	Pass ± 2 kV
ESD – Charged-device model (CDM) rating JS-002-2018 (Total samples from one wafer lot)	3	Pass ± 350 V – Jedec Class C1. ▪ VSS_BT (pins C2, D2, D3, E1, and E2), BT_RF (pin D1), and VDD_BT_1V8 (pin F1) pass 350 V ▪ Other pins pass 500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	6	Passed
Latch-up (V-supply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 85°C (Total samples from one wafer lot)	6	Passed

[a] Combined data from 2 variants of the same device for calculation.

22.2 Package reliability results

Table 22-2 Package reliability results

Tests, standards, and conditions	Sample size	Result
Moisture resistance test (MRT): J-STD-020-n Reflow at 260 +0/-5°C (Total samples from four different assembly lots)	240 x 6 lots	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to 125°C Number of cycles: 1000 Soak time at minimum/maximum temperature: 8-10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-G MSL 1, reflow temperature: 260 +0/-5°C (Total samples from four different assembly lots)	80 x 6 lots	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113-G MSL 1, reflow temperature: 260 +0/-5°C (Total samples from four different assembly lots)	80 x 6 lots	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration Preconditioning: JESD22-A113 MSL 3, reflow temperature: 260 +0/-5°C (Total samples from four different assembly lots)	80 x 3 lots	Pass
High-temperature storage life: JESD22-A103 Temperature 150°C, 1000 hours (Total samples from four different assembly lots)	80 x 6 lots	Pass
Flammability **NOTE** Flammability test – not required UL-STD-94 Qualcomm Technologies, Inc. (QTI) ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	See the note under the Tests, standards, and conditions column.
Solder ball shear: JESD22-B117 (Total samples from four different assembly lots at each SAT)	Spec: > 220 g Avg: 340 g	Pass

Tests, standards, and conditions	Sample size	Result
Wire pull MIL-STD-883E, Method 2011 (Total samples from four different assembly lots at each SAT)	Spec: > 6 g Avg: 13.36 g	Pass
Wire ball shear: JESD22-B116 (Total samples from four different assembly lots at each SAT)	Spec: > 12 g Avg: 25.21 g	Pass

22.3 Board level reliability results

Table 22-3 Board level reliability results

Tests, standards, and conditions		ASE
Drop test: JESD22-B111 1500 G, 0.5 ms, 200 drops	Sample size:	120
	Failures:	0
	First fail:	n/a
Temperature cycle: JESD22-A104D Temperature: -40°C to 125°C; number of cycles: 1500 Soak time at minimum/maximum temperature: 15 minutes Cycle rate: 1 cycle per hour (CPH)	Sample size:	30
	Failures:	5
	First fail:	1790 cycles
	η (63.2% failure rate):	2058 cycles

NOTE Data is leveraged from another device with the same package technology (144VFBGA, 7.5 x 7.5 x 1.0 mm, 0.5 mm pitch).

Document references

Document	Reference, date
Bluetooth Core Specification	Bluetooth Specification Version 5.4, 31 January 2023
Bluetooth v5.4 RF-PHY Test Specification	Bluetooth Test Suite Version RFPHY.TS.p19, 07 February 2023
ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level	JS-001-2017
ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Device Level	JS-002-2018
I²S Specification	Revised: June 5, 1996. Philips Semiconductors
IC Products Packing Method	80-VK055-1
QCC3095 VFBGA Hardware Design Guide	80-74170-1
Typical Solder Reflow Profile for Lead-free Devices Information Note	80-CT462-1

Glossary

Term	Definition
ADC	Analog-to-digital converter
ADK	Audio development kit
AIO	Analog input/output
ANC	Active noise cancellation
B/W	Bandwidth
BAC	Buffer access controller
Balun	Balanced/unbalanced interface or device that changes a balanced output to an unbalanced input or vice versa
Bluetooth	Set of technologies providing audio and data transfer over short-range radio connections
BTL	Bridge-tied load
codec	Coder decoder
CPU	Central processing unit
DAC	Digital-to-analog converter
DMA	Direct memory access
DSP	Digital signal processor (or processing)
ESD	Electrostatic discharge
HQ	High quality
I/O	Input/output
IC	Integrated circuit
IDE	Integrated development environment
IQ	In-phase and quadrature
I²C	Inter-integrated circuit interface
I²S	Inter-integrated circuit sound
kpcs	Thousand pieces
LDO	Low (voltage) drop-out
LED	Light-emitting diode
MCLK	Audio master clock
MIB	Management information base
MIPS	Million Instructions Per Second
MMU	Memory management unit
MSL	Moisture sensitivity level
NSMD	Nonsolder mask defined

Term	Definition
NTC	Negative temperature coefficient thermistor temperature monitoring circuit
OEM	Original equipment manufacturer
OTP	One-time programmable
PCB	Printed circuit board
PCM	Pulse code modulation
PIO	Programmable input/output, also known as general-purpose I/O
PMU	Power management unit
PWM	Pulse width modulation
QMDE	Qualcomm® MultiCore Development Environment
QSPI	Quad serial peripheral interface (flash)
QTIL	Qualcomm Technologies International, Ltd.
RAM	Random access memory
RF	Radio frequency
RISC	Reduced instruction set computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/ EC)
ROM	Read only memory
SDR	Single data rate
SMPS	Switch-mode power supply
SNR	Signal-to-noise ratio
SoC	System on-chip
SPDIF	Sony/Philips digital interface
SPI	Serial peripheral interface
TCM	Tightly coupled memory
THD+N	Total harmonic distortion plus noise
UART	Universal asynchronous receiver transmitter
ULP	Ultra low power
USB	Universal serial bus
USB-FS	Full speed USB
VSWR	Voltage standing wave ratio
XTAL	Crystal

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